Reliable High Density Stacked Memristor Memory Designs

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***Abstract*—A conventional design has an insulator layer for every crossbar layer stacked. Methodology for alternatively selecting memristor layers and methodology for proper operation are proposed. It would help increasing the vertical density of stacked memristor crossbar arrays. It is the maximum possible memory density design for crossbar stacks. While still suffering a few shortcomings, concurrent access in particular, the new design proves itself as an interesting design alternative because of increase in memory density. For a 2 nm insulator thickness in conventional design, at least 27.50 percentage increase in vertical crossbar density is expected in the proposed design. Alternative designs and approaches have also been proposed to address the shortcomings.**

***Keywords*—Random access storage; very-large-scale integration (VLSI); analog circuits**

I. INTRODUCTION

A higher bit density in computer memory could help many portable devices, implantable devices, and with higher reliability it can help IoT (Internet of Things) hardware. It can save material costs. This is one such an effort where the memory density is increased across stacked crossbars. The height/thickness in general is not seen critical on 3D stack memory where each layer is stacked, but with the proposed extrapolated designs, the vertical memory density i.e. height/thickness is comparable to the lateral dimension because of significant increase in vertical memory density. In some cases (like when there is no separate insulation material used to separate each memristor cells), the vertical density is higher than the horizontal i.e. in each stacked crossbar density. So it becomes important to value the vertical height/thickness, especially for applications like smaller portable devices, more choices in physical dimensions for implantable devices and reducing cost as well.

The density of [24] could be similar to that of the proposed design. But there are two important differences. First, the key aspect of [24] to have reverse material design on adjacent crossbar layers is not a necessity in the proposed design, material order can be reverse or can be same order for adjacent layers. Second, the need for dynamic insulation during operation is important in the proposed design. An active column and row is called as the primary crossbars; other rows and columns are called as secondary crossbars. Thus, three unselected memristors in a path is called as Dynamic Insulator. The key advantage of dynamic insulation is the reliability it offers during read and write operations for concurrent access, which is important for IoT hardware. It is the combination both the design and dynamic insulation makes this proposal a better model. In a conventional 3D memory integration of memristors like in [7], layers of crossbars are stacked on top of one another on a substrate and each layer is separated by a layer of insulator. When the crossbar layers are separated from one another with insulator layer in-between, each crossbar layer has row and column bars with memristor layer [10] in-between them as shown in Fig. 1. Comparing further with other state-of-the-art 3D stack conventional designs [14], [20], [21], the proposed designs are still of higher memory density, since the conventional designs still include the insulator layer across crossbar stacks. Since the proposed design has only the crossbar layers and the memristor cells, it makes the maximum possible memory density for crossbar stacks.

In this study, TiO_2 and oxygen-depleted TiO_2 i.e. TiO_{2-x} is considered as the term 'Memristor layer'. In the proposed designs, instead of using an insulating layer and having two separate crossbar layers, each crossbar is shared across two adjacent memristor layers. In other words, a methodology for alternatively selecting memristor layers and a methodology for proper operation is proposed so that it would help increase the vertical density of stacked ReRAM (Resistive Random-access Memory) crossbar arrays. Thus, there is increase in overall density by saving the space of an insulator layer and a crossbar layer and saving cost on related materials. The insulation is created by making use of a dynamic insulator method that's explained in the following sections. However, there is trade-off on concurrent access, and alternative methods are also proposed to further mitigate the effect of already small tradeoff.

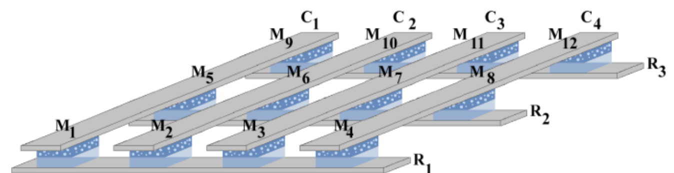


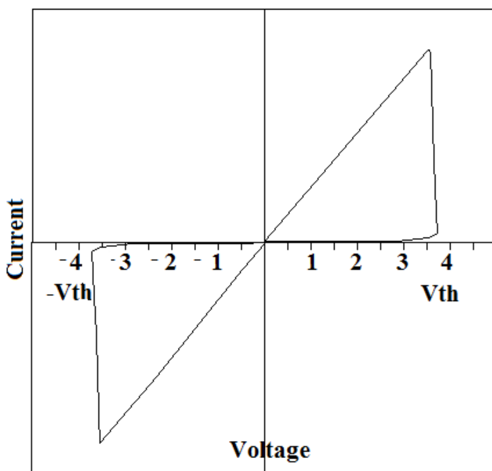
Fig. 1. A generic crossbar structure. It has 12 memristor cells. TiO_2 is typically transparent as shown.

The proposed designs are not limited to these materials; it's expected to work with any similar memristic devices which work on single layer crossbars. In Fig. 1, C_1 to C_4 are four column bars, R_1 to R_3 are three row bars and M_1 to M_{12} are the twelve memristors. The cross-points between the column and row bars are called the memristors. It's because only the region of memristor layer that is in-between the cross-points undergoes state change. Other regions in-between the cross-bars can be the same memristor layer or it can be an insulator.

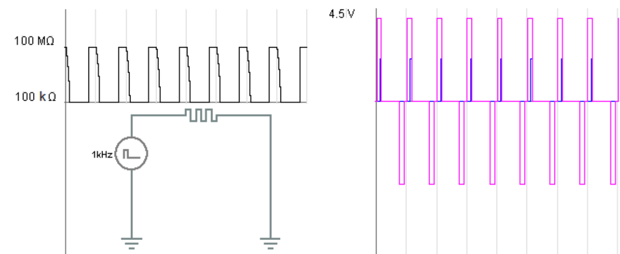
When the selected memristor is externally applied with voltage above the threshold voltage, it's programmed ON [8], [19]. The current-voltage characteristic of memristors can be non-linear as shown in Fig. 2(a), that is, the change of memristance is exponential above threshold voltage but negligible for below threshold voltage when applied for a limited period. All other memristors below the threshold voltage are not programmed ON.

For example, if the memristor M_6 in Fig. 1 is to be selected and the threshold voltage is V_{th}, then crossbars C_2 & R_2 are applied with voltages $+(V_a/2)$ & $-(V_a/2)$ or $-(V_a/2)$ & $+(V_a/2)$ respectively so that potential across the selected memristor is V_a. V_a should be greater than V_{th} but $(V_a/2)$ is lesser than V_{th}. Since C_2 and R_2 direct cross-point is at M_6, this memristor is programmed ON. All other memristors are below threshold voltage so they are not programmed ON. Taking the case of memristor M_{10}, though it's in the path between the two cross bars C_2 and R_2 via C_2, M_{10}, R_3, M_{11}, C_3, M_7 and R_2, it's still unselected because of voltage drop across different memristors in the path would bring the effective voltage applied on it below threshold voltage. This is the case for all unselected memristors. It can be noted that for all unselected memristors each memristor has a path between C_2 and R_2 with at least three memristors between the primary row and column. The active C_2 and R_2 is called as the primary crossbars; other rows and columns are called as secondary crossbars. Thus, the three unselected memristors in a path is the Dynamic Insulator.

Corollary 1: There is voltage drop across the memristor(s). This is true for memristors that would have resistance even at low resistance state because of TiO_2 layer.



(a)



(b)

Fig. 2. (a) An illustration of hysteresis loop. The state of memristance can change on reaching V_{th}, otherwise negligible. (b) An example simulation to show change in memristance for selected memristor for +/- 4.5 V across the selected memristor.

II. Proposed Stack Structure

The dynamic insulator observed in a single crossbar is extrapolated to a 3D crossbar stack structure. Fig. 3 illustrates the proposed 3D crossbar stack where row and column bars are placed alternative to each other, each separated by a memristor layer, as a stack.

When the crossbars are placed as a stack with memristor layers in-between them, the bars are shared between the neighboring memristor layers on the top and below. This helps in saving vertical space. It's because when three layers of memristor in stack are not programmed ON, they would act as an insulator in-between two other active memristor layers.

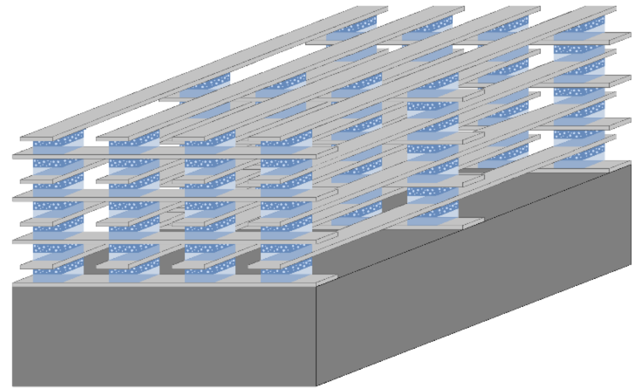


Fig. 3. Proposed 3D crossbar stack structure. This structure is detailed with notations in Fig. 4.

These three non-active memristor layers could be called as a Dynamic Vertical Insulator as shown in Fig. 4(b). Thus, one could have two active crossbars for every dynamic vertical insulator layer of three memristor layers in-between them. The working principle of the dynamic vertical insulator is explained in Section V.

The Fig. 4(a) is the top view of the crossbar stack. The different device structures are marked with their names. For example, $M_{1\ (i...vii)}$ refers to seven vertical layers of memristors where M_{1i} would be the memristor at the bottom of the stack, next-above the substrate. Similarly $C_{1\ (i...iv)}$ are for the four vertical column bars beneath one another, C_{1iv} being the top-most column and $R_{3\ (i...iv)}$ refers to the four vertical row bars beneath one another. Thus, in the given names, 'i' would be the layer just above the substrate, 'iv' would be for the top-

most row and column bars and 'vii' would be for the top-most memristor in the stack. The arrow in the figure indicates the direction of the front view of the structure. Fig. 4(b) and 4(c) are the front and side views of the stack. Fig. 4(b) is similar to Fig. 4(a) to (c) except that the crossbars are rotated by 90 degrees so that there are lesser number of interconnects that would be used to communicate between crossbars and buried CMOS switches similar to [9], [12].

Concurrent and independent access between successive layers is difficult in the stacked 3D crossbar. For example, if memristors M_{1v} and M_{1vii} are to be selected, then memristor M_{1vi} would be disturbed. In addition to this problem, considering another case, when M_{5vi} and M_{5vii} are to be changed to low resistance state i.e. written with '1' bit, the voltage would be in opposite directions i.e. if M_{5vi} would have $-(V_d/2)$ at R_{2iv} and $+ (V_d/2)$ at C_{1iii} then M_{5vii} would have $-(V_d/2)$ at R_{2iv} which is in opposite polarity for M_{5vii} and would need a $+(V_d/2)$ to program it ON. Thus, the polarity dependence of memristors would change the state of these two memristors each in the opposite directions. So, defining alternate layers to represent high resistance state as '0' bit in one layer and '1' bit in the next layer and similarly low resistance state as '1' bit in one layer and '0' bit in the next layer would be a complex overhead.

The extrapolated dynamic vertical insulator method is expected to work because the unselected memristors across three inactive layers would have the same effect of the unselected memristors in a single layer crossbar. So the effective voltage applied across the unselected memristors in each of the three vertical layers would be in the safe region which is well below threshold voltage. Thus, random access within each active layer is possible.

Let the memristors M_{1i} and M_{1v} be selected at the same time. For this condition, the crossbars C_{1i}, R_{1i}, C_{1iii} and R_{1iii} needs to have voltage applied to it. All other bars are floating. Let C_{1i} and C_{1iii} be applied with $+(V_d/2)$, and R_{1i} and R_{1iii} be applied with $-(V_d/2)$. This would program ON memristors M_{1i} and M_{1v}. So layers M_i and M_v are the active layers. Layers $M_{(ii\text{-}iv)}$ is expected to behave like an insulator and is analyzed in this section.

In this stack there are 84 memristors in total of which 2 are selected. To analyse the cases of unselected memristors, $M_{5i\text{-}vii}$, $M_{12i\text{-}vii}$, $M_{1ii\text{-}iv}$ and $M_{3i\text{-}vii}$ are considered. Considering these memristors should suffice for 82 unselected memristor cases because they represent the groups: 1) Memristors in the active crossbar layer with one primary crossbar in direct contact; 2) Memristors of adjacent layer with one primary crossbar in direct contact; 3) Memristors in the active crossbar layer with no primary crossbar in direct contact; 4) Memristors in inactive layers with no primary crossbars; 5) Memristors in the same column of the two concurrently selected memristors.

Taking the case of $M_{1(ii\text{-}iv)}$, it's in-between primaries C_{1i} and R_{1iii}. Since C_{1i} and R_{1iii} are applied with voltages $+(V_d/2)$ & $-(V_d/2)$ or $-(V_d/2)$ & $+(V_d/2)$ respectively, the voltage drop across each of the three memristors would make the effective voltage applied on each of these memristors less than threshold voltage. Since memristors $M_{1ii\text{-}iv}$ are unselected, this should be the case for any of the memristors in layers M_{ii}-M_{iv}.

Memristors of M_i and M_v layers are the unselected memristors of the active layers, hence applying the condition of unselected memristors of single layer, these memristors would be below threshold voltage, considering M_i and M_v are separated by M_{ii}-M_{iv}. Memristors of M_{vi} and M_{vii} layers are further away from layer M_i, so they would be well below threshold voltage.

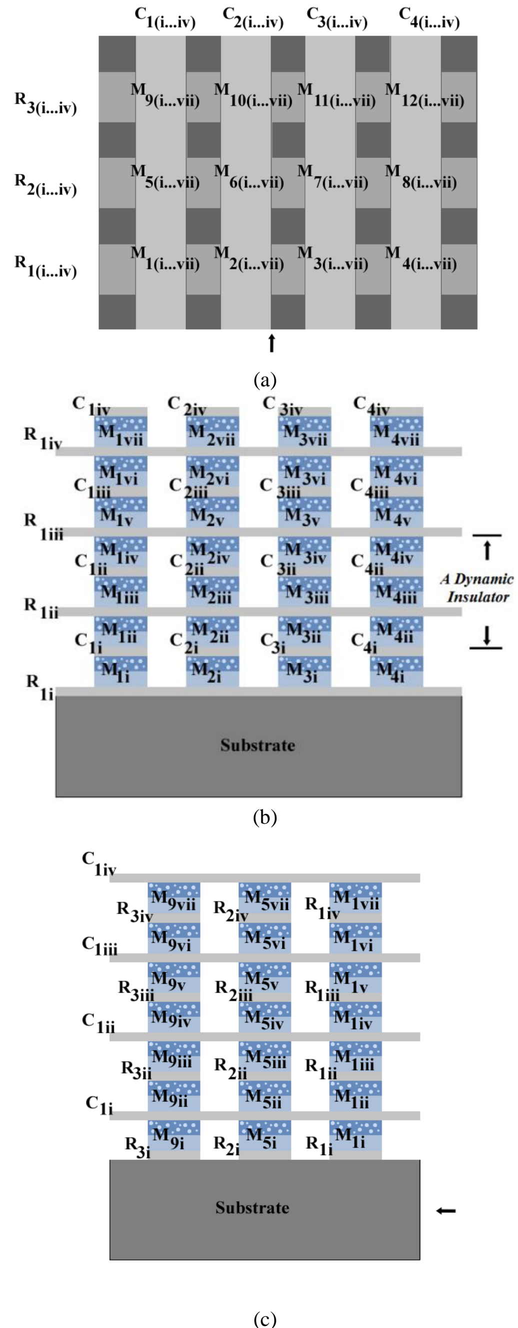


Fig. 4. (a) Top-view of 3D crossbar stacks structure. The arrow indicates the direction of front-view. (b) Front-view of 3D crossbar stacks structure. (c) Side-view of 3D crossbar stacks structure. The arrow indicates the direction of front-view. (d) The crossbar layers is rotated by 90 degrees so that one side of the crossbars is directly connected to the substrate. This is an alternative way

of making the interconnects with the control circuits that would need to communicate to the buried CMOS switches in the substrate.

Thus, for each of the unselected memristors there are at least three memristors in the path between any of the primary crossbars; there is resistance for a memristor even at a low resistance state from *corollary 1*. So, the effective applied voltage would be less than the threshold voltage for any of the unselected memristors. Hence, there would be no change in their state of memristance. Three vertical memristor layers $M_{(ii\text{-}iv)}$ are considered for a dynamic vertical insulator.

In comparison with conventional design, [7] can have all its crossbar layers active at the same time at peak performance while this design needs to have three inactive crossbar layers for every active crossbar layer. In another way of looking at it, the layers that are active concurrently can be grouped as memories I, II, III and IV. Thus for each of the memories, their memristors can be accessed randomly within the layers and across the layers but when one memory is accessed, layers of other memories are inactive. This can be reduced to three memories I, II and III for a 2 layer dynamic insulator thickness.

III. Conventional VS Extrapolated

The memristors that are fabricated by different research teams is surveyed. Their thickness is compared with the density of conventional 3D crossbar design against the extrapolated design and is plotted in Fig. 6. The thickness of memristor A [1] is Ag (200 nm) TiO_{2-x} (20 nm) TiO_2 (2 nm) ITO (200 nm), B [2] is 15 nm each of Ti/Pt TiO_{2+x} TiO_2 Ti/Pt, C [3] is Pt (50 nm) Ti (5 nm) TiO_2 (4 nm) TiO_{2-x} (110 nm) Pt (50 nm) Ti (5 nm), D [4] is $Metal_2$ (800 nm) TiO_{2-x} (220 nm) TiO_2 (450 nm) $Metal_1$ (500 nm), E [4] is $Metal_2$ (800 nm) TiO_{2-x} (50 nm) TiO_2 (50 nm) $Metal_1$ (500 nm), F [5] is Ti (5 nm) Pt (15 nm) TiO_2 (30 nm) TiO_{2+x} (30 nm) Ti (5 nm) Pt (15 nm), and G [6] is Pt (80 nm) Ti (5 nm) TiO_2-bilayer (50 nm) Pt (80 nm) Ti (5 nm).

Tabulating the value resistances for these devices is limited to theoretical values known otherwise from [23]. The resistivity of TiO_{2-x} layer is calculated into resistance for an illustrative lateral dimension 50 nm x 50 nm and 15 nm thickness as shown in following Fig. 5. In this figure, only 3.7 x 10^{18} cm^{-3} and 8.5 x 10^{18} cm^{-3} are considered for oxygen deficiencies from [23] since the figure is only to illustrate for the variations of 'x'.

The thickness of the insulator for the conventional design [7] is considered with a low value of 2 nm in Fig. 6(a). This insulator thickness is expected to be considerably more in a practical implementation for any of the listed memristors. However, comparing the density for 2 nm thickness should at least set a benchmark for any other larger value. A larger insulator thickness would decrease the density of only the conventional design because the extrapolated design does not have insulator layers in-between crossbars and the comparative density increase is illustrated in Fig. 6(b).

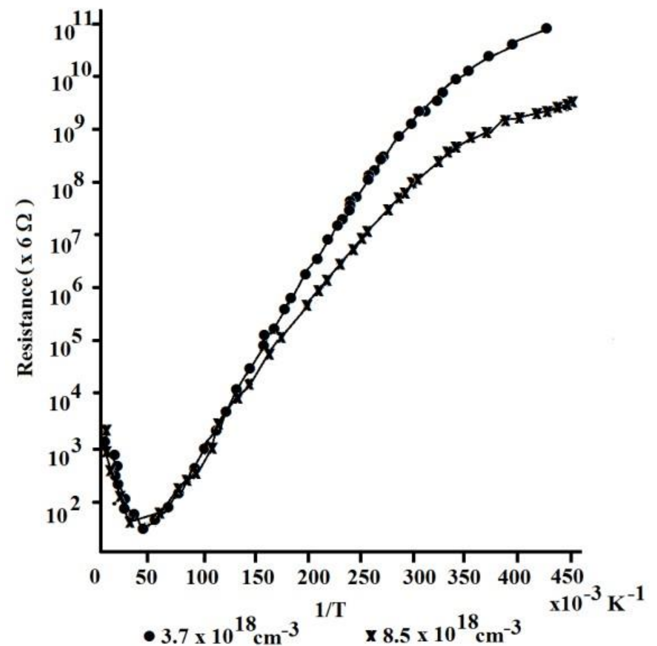
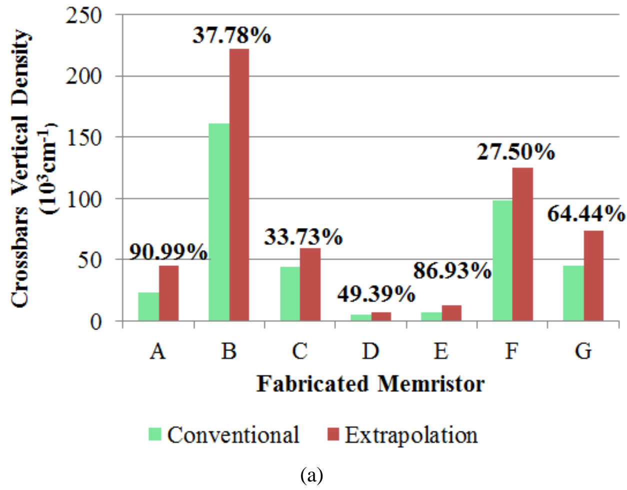


Fig. 5. The x-axis is the inverse temperature and y-axis is the resistance. The two curves are for two different oxygen deficiencies of TiO_{2-x} from [23].

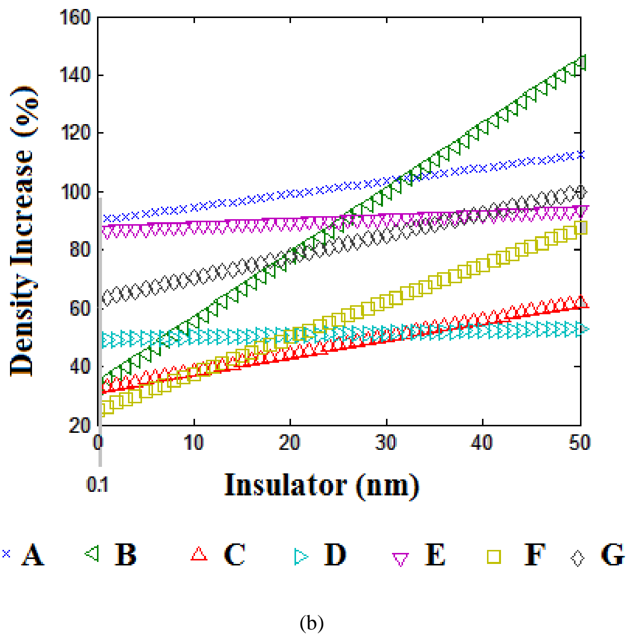
From Fig. 6(a), it could be observed that there is considerable increase in crossbar vertical density using the extrapolated design for different memristors, the density increase ranges between 27.50% and 90.99% for a 2 nm insulator thickness in the conventional design [7]. This percentage is higher for insulator thickness larger than 2 nm as shown in Fig. 6(b). The insulator thicknesses are from 0-50nm. This figure is to show the percentage increase in density for extrapolated design against conventional design that has insulator layers. There is increase in density for increase in insulator thickness because the extrapolated design does not have insulator layers. It's the conventional design that has insulator layers. So comparing conventional design and extrapolated design against the increase in thickness for insulator layers, there is decrease in density for conventional design. Thus there is increase in density percentage for extrapolated design when compared to conventional design [7].

The proposed design can be further extrapolated to address high-bandwidth and low-latency in communication issues by hardly trading off the higher density it has over other state-of-the-art designs [14], [20], [21]. Fig. 7(a)-(d) illustrates for a single tile, step-by-step, how each cross bars are stacked. Similar tiles can be arranged on the dorsal and ventral sides of this tile. The number of crossbars and interconnects on each tile is not limited to as shown in Fig. 7. The different colors for the metals in Fig. 7, (red, green, orange and dark grey and light grey) are only to illustrate the different layers each metal

serve, however it can be the same material of metal for all them. The light and dark grey metals are the crossbars and their intersection makes a single memristor cell. The red metal bars are connected to each stack layer independently whereas the green metal bars are shared across stacked layers. However, the green bars can be replaced with independent red metal bars to have more independent control of each stacked layer but doing so would increase lateral dimension as there would more red metal bars.



(a)



(b)

Fig. 6. (a) Comparison of Cross-bars vertical density between conventional and extrapolated designs. The percentage shown in the figure is the increase in crossbar vertical density percentage with extrapolated design in comparison to a conventional design. The height of the stacked memristor is the criterion. (b) Increase in density for extrapolated design against conventional design for insulator thicknesses 0.1-50 nm in conventional design. It is not from 0 nm because at 0 nm the conventional design can either be regarded as the extrapolated design or have only contact resistance that's negligible for this study, while even the 0.1 nm may be too thin to be a reliable insulator.

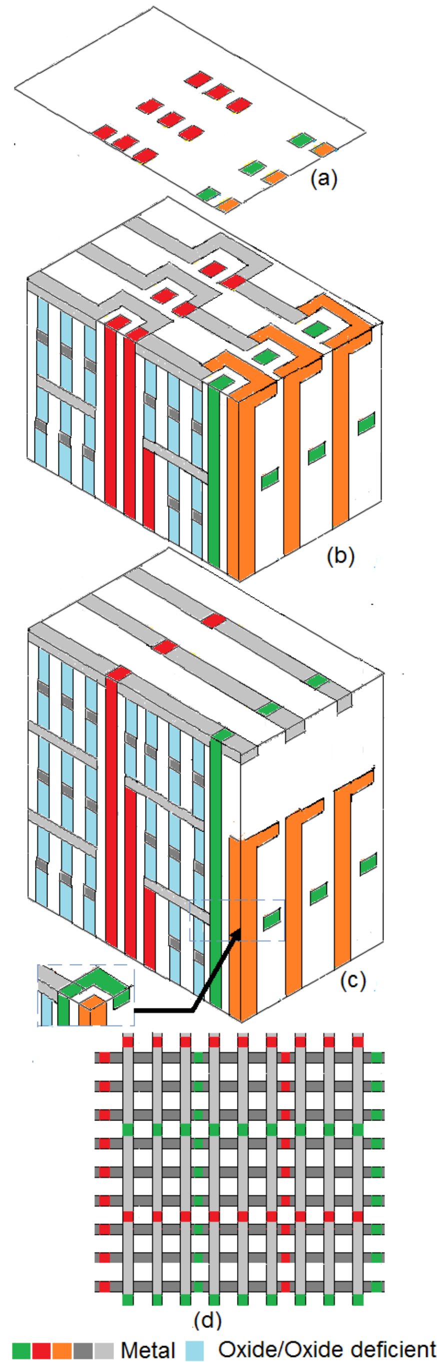


Fig. 7. (a) Cross-section at the interface that connects to the buried CMOS. The rectangles filled with colors red, green and orange are the metal bars. (b) Cross-section on top of one of the crossbar layers. (c) Isometric view at the top most crossbar layer. It also shows a snippet of the pattern in another crossbar layer. (d) Top-view of multiple tiles arranged alongside.

A single functional unit of stacked crossbars would have red metal on two sides and the green metals on the other two sides as shown in Fig. 7(d). Hence, these red and green metals are shared with other neighboring functional units as shown in

that figure. Increasing of number of the layers will significantly increase the fabrication cost. But when column/row lines length increases, there is no additional increase in the number of layers and that can be seen through Fig. 7(d). When accessing one functional unit, it is expected that all other functional units are not turned on. However, other functional units can be turned on such that it does not affect the desired operation of any other functional unit. The voltage in metal bars of these functional units can be compared to resistor networks and hence, controlled accordingly with desired voltages with the help of buried CMOS switches. So to address a memory cell, one needs to know the tile, stacked layer and the cell that needs to be accessed.

The following two approaches are intended to increase the speed of read/write access:

A. *Twin Row/Column Access*

In a row read/write, like in [11], in a single layer crossbar in Fig. 1, for row R_1, memristors $M_{1\text{-}4}$ can be selected by first applying voltage at R_1 and grounding or applying voltage across each column C_1-C_4 each at a time. In a 3D stack in Fig. 3, for a single row selection of R_{1ii}, column layers C_i and C_{ii} can be applied with voltage with one column at a time. Thus, for a single row crossbar selection, two layers of memristors in a 3D stack can be accessed by changing across the column bars. Concurrent access of two columns would be a better read because of the x2 speed, however, the density might be half of the initial proposed design.

B. *The hybrid Zebroid design*

In the hybrid design, layers of extrapolated design crossbars are stacked on top of each other and followed by an insulator layer as in conventional design. Then again a number of extrapolated layers can be stacked on top of them.

This would give a higher density than conventional design and higher concurrency than extrapolated design, whilst lower density than extrapolated design and lower concurrency than conventional design. The number of layers between conventional and extrapolated can be determined according to the application.

Fig. 8. Front-view of Zebroid stacks. The advantage of this design is have the option to choose between higher density and concurrent access as needed.

Fig. 8 illustrates a hybrid design. To keep fabrication steps simple, the insulator layer can be only TiO_2 but of appropriate larger thickness than other TiO_2 layers. In case, the application of RRAM crossbars would be for implantable devices, it is always better to have as many choices as possible, considering need for accurate size and concurrent access. But for such application specific need of choices, the hybrid design can be trivialized compared to extrapolated design.

So the optimal balance of configuration between concurrent access and high density is entirely application specific.

IV. Simulation Analysis

The voltage applied across the memristors is the main principle for dynamic veritcal insulator. *Falstad* simulator [13] for electronic circuits is used for simulations. This simulator is not specific to any model but it does generic memristor circuit simulations considering equations that define a memristor. For this analysis, this simulator would generate the needed data. Fig. 9 is a simulation of conventional memristor crossbar network.

The layers are connected such that concurrent read and concurrent same-bit writes are possible. In Fig. 10(a), memristors have design similar to Fig. 3 and named as in Fig. 4.

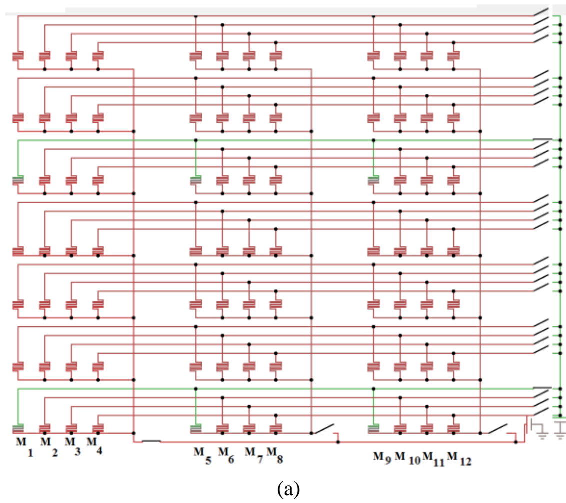
The concerned values for this analysis is the high resistance state and low resistance state and they are set as 100 MΩ and 100 kΩ. In the conventional design, at first instance time of 5 µs when all the memristors are at their default value, for +/- 4.5 V i.e. -/+2.25 V and +/-2.25 V in both directions, the power dissipation for sum of all memristors is 1.063 µW and 1.063 mW when all 84 memristors are at 100 MΩ and 100 kΩ, respectively.

Similarly for extrapolated design, the power dissipation is 1.325 µW when all 84 memristors are at 100 MΩ and it would be 1.325 mW when all 84 memristors are at 100 kΩ. There will be change in potential, current and power dissipation across unselected memristors for changing values of memristance with time.

There is an increase in power dissipation for the extrapolated design but it's in low range. Also, the number of crossbars is lesser for extrapolated design, so the power dissipation on the crossbars is expected to be lesser than on the conventional design.

The voltage across the selected memristors will be above threshold voltage so they would be programmed ON. When the threshold voltage is reached, the memristor would change its state according to the sign of voltage and polarity. Since the memristance change would also be time dependent, access should be for a limited duration. Memristors are polarity dependent, so they would become more conductive for positive potential and more resistive for negative potential.

Switches (non-memristors) are shared across layers. But having separate switches to access individual layers is expected to give better concurrent access since positive and negative voltages can be applied to independent memristors while adding switches would take additional space.



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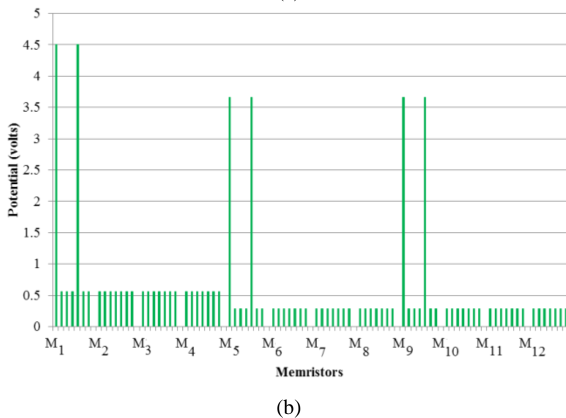
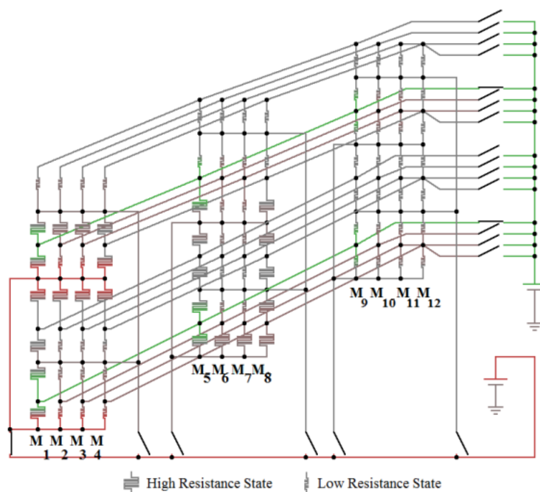
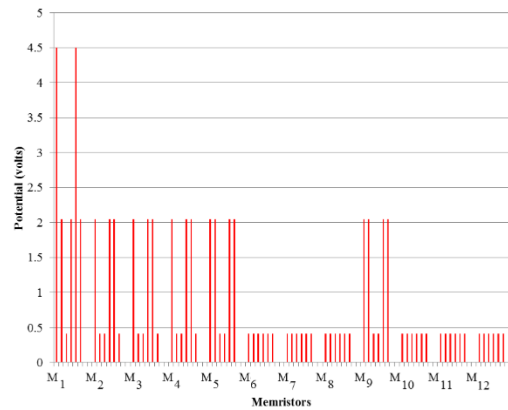


(b)

Fig. 9. (a) Simulation of memristor crossbar network of conventional design, all memristors are in high resistance state. Since this figure is a simulation screenshot, this figure may not be visually inviting to read. (b) Magnitude of potential across memristors of conventional design for two active layers separated by three layers in-between as in (a).



(a)



(b)

Fig. 10. (a) Simulation of memristor crossbar network of extrapolated design, memristors are in high and low resistance states. B. Magnitude of potential across memristors of extrapolated design for two active layers separated by three layers in-between as in (a). When comparing Fig.9(b) and 10(b), the voltage for unselected cells are different and it is not better for extrapolated design than the conventional design but it is below by a significant value to consitute for below threshold voltage values.

V. SNEAK CIRCUIT ANALYSIS

In the stack memristors are the devices to consider. All other devices in the network are computational and instrumentation elements, so in editing they are removed from traced paths. A read signal with a negative pulse followed by a positive pulse with equal magnitude and duration should be able to read the state of a memristor [16], with voltage above threshold voltage. The width of the pulse and magnitude is such that it doesn't change the state of memristor after a read cycle. This would not affect the state of memristors in sneak path because of the polarity dependence of memristors; the positive pulse would annul the change by negative pulse, when the widths and magnitudes are equal for the two square pulses.

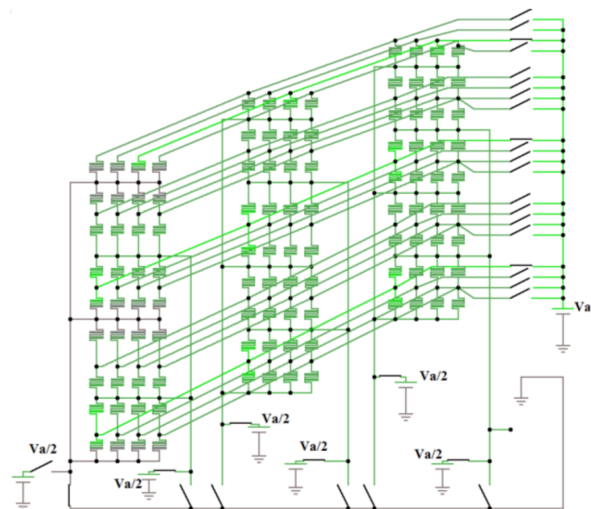


Fig. 11. Extrapolated design simulation with Sneak Path Protecting Voltages.

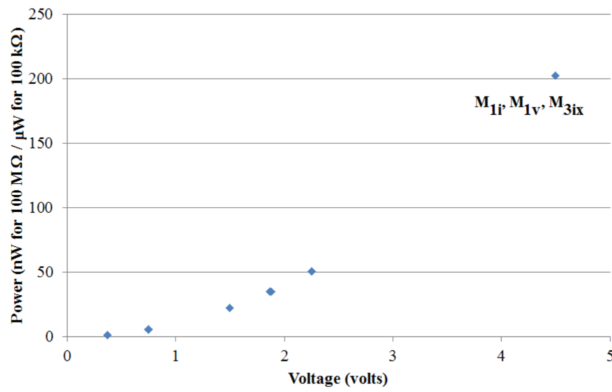


Fig. 12. Magnitude of Voltage and power of 108 memristors in Fig. 11. The memristors are initially at 100 MΩ/100 kΩ.

In write operation, there could be sneak paths because of which the unselected memristors could have voltage above threshold voltage. To increase number of concurrent access the unselected memristors are applied with $V_a/2$ voltage in the opposite direction, as shown in Fig. 11, so that the maximum voltage across unselected memristors would not be above $V_a/2$. For simulation analysis in Fig. 11, the number of memristor layers is increased to 9 layers from 7 layers in Fig. 10(a), so three concurrent active layers can be studied for potential and current across. It's only the selected memristors have both terminals' to primary crossbars.

Secondary voltage terminal have voltage lower than primary terminal because of voltage drop across memristor(s). All unselected memristors have at least one secondary voltage terminal. Thus, applying a $V_a/2$ or selective higher voltage in the opposite direction should have the unselected memristor(s) to a maximum voltage of only $V_a/2$ or below, so the unselected memristors would be lesser than threshold voltage. V_{th} is given by $V_a > V_{th} > V_a/2$.

Fig. 12 illustrates the magnitude of potential and power across the 108 memristors. In the simulation, the measurements were noted at 5 µs when all the memristors are at their default value of 100 MΩ. First a single active crossbar was tested and only one memristor M_{5V} was selected in the network and all other memristors were either unselected for both crossbars or applied with counter balancing potential $V_a/2$ to eliminate possible sneak paths. The highest potential was $V_a/2$ for unselected memristors. Fig. 9(a) illustrates for two concurrent active layers where only the selected memristors M_{1i} and M_{1iv} are at V_a and all other unselected memristors are below $V_a/2$ as shown in Fig. 9(b).

When resisters were considered in Fig. 10(a) instead of memristors, for a single resistor selection for the network the highest potential across unselected resistor was 2.91 V for applied V_a of 4.5 V across the single selected resistor and counter-balancing potential was not applied to unselected resisters. Next step is to study three concurrent memristors, so M_{1i}, M_{1v} and M_{3ix} were selected in the network in Fig. 12. As determined, only the selected memristors were having the highest voltage, current and power. For example, the unselected memristors have voltage below 2.25 V for applied 4.5 V. The selected memristors have 4.5 V. Also, the unselected memristors have voltage below threshold voltage i.e. below 2.25 V for one, two or three active crossbar layers for the design in Fig. 11. Fig. 12 was simulated for when all memristors are at initial state of 100 MΩ. The power is in nW, and since its similar to a resistor network it would be in µW with corresponding numbers when all memristors are at initial state of 100 kΩ. Thus, it would work for bipolar memristor devices. The current magnitude in selected memristers was at least twice more than unselected memristors as derived from Fig. 12. Also, the alternative techniques [22] that handle sneak current give scope for unipolar memristor devices as well.

Thus, from the above analysis, it's possible to read and write [16], [22] to selected memristors in the extrapolated designs. Also, zero or reverse bias will also help in minimizing sneak current further in cells in dynamic isolation layers.

VI. Conclusion

Since the three non-active memristor layers act as dynamic vertical insulation, the operation of it would require designing additional circuit to control it. So there will be additional power overhead. Further quantification of the reliability will require fabrication of the proposed designs, and it is the next step forward for this work. Only such experimental data can evaluate the real effectiveness of the proposed designs in terms of leakage current, data patterns, understand the fatigue of memristors when disturbed many times, speed, material and sheet resistance in detail. Also, this simulation analysis is with a R-ratio of 1000. But it would be an interesting experimental analysis if the R-ratio would be less than 100 for read operation analysis against sneak current. Though there are limitations to concurrent access when compared to conventional design, this design still has higher density as shown in Fig. 6. Since this study has shared non-memristor switches for computational and instrumentation elements across layers, having separate switches to access individual layers should give better access. Since the number of crossbars is lesser for extrapolated design, the power dissipation on the crossbars is expected to be lesser for extrapolated design than it would be on the conventional design. The dynamic insulator thickness could further be reduced to two memristor layer thicknesses, thus facilitating more concurrent access; this requires further investigation.

The hybrid design would give higher concurrency than extrapolated design and higher density than conventional design but a lower density than extrapolated design and lower concurrency than conventional design. The number of layers in-between could be application dependent. However, it needs to be seen how much impact would high density of vertical interconnects would make the difference between the designs, especially the need for higher bandwidth and lower communication latency.

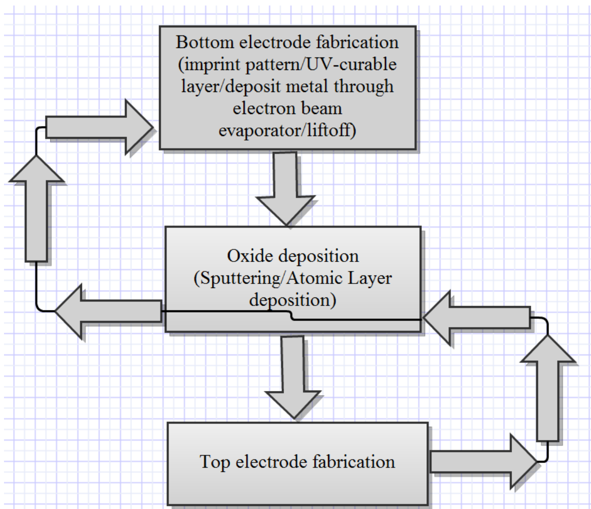


Fig. 13. Generic Nano-Imprint Lithography with flow for stack fabrication, each iteration is would make a crossbar pair with a memristor layer.

Some applications have been identified as where this design approach would be useful. The RRAM stack design's niche is for applications that would read more than write [7]. In Field Programmable Gate Arrays the need to have large programmed data would greatly benefit from this design. Portable memory devices especially those used for IoT hardware that require high reliability and Synapses in neuromorphic circuits would need high connectivity and high density [15] and it's where the hybrid design could be desired than the extrapolated.

This work can be extended in the following ways in future.

A. Develop Advanced Simulator

There could be program disturb concerns during SET/RESET operations. Hence, there is need to develop the simulator [13] further so that additional disturb issues in dynamic insulators can be studied, by simulating complex read and write operations, stored bit patterns, and also study energy for each operation.

B. Fabrication of Extrapolated Design

The proposed designs are being fabricated in laboratory to further verify the simulation results and serve as a prototype. In Nano-Imprint lithography (NIL) [18], electron beam lithography, photolithography and reactive ion etching steps are followed. The flowchart in Fig. 13 briefly illustrates the generic processes in NIL and flow for crossbars stack fabrication. As shown in the flowchart the steps are an iterative process where the number of iterations depends on the number of crossbars stacked. Kinks on the metal wire (crossbar) like in [17] are not desirable since the layers would be stacked. The stack would require a planar structure for metal wires. Thus, a planer oxide deposition should help to fabricate a planar top electrode so further layers could be stacked on top.

C. Data Storage Optimization

Data can be stored in various arrangements of bits across multiple crossbars. It is desirable to access related bits concurrently during read/write so that overall read/write time for related information is less. The planned work is to determine how the bits are arranged for storage across multiple crossbars so that it maximizes concurrent read/write access and thus, minimizes overall read/write time for a set of bits.

D. Interconnects Latency, Bandwidth and Size

Even though the proposed designs are of higher memory density than the conventional designs [7], [14] and give room to be used in applications such as portable memory devices, it will be interesting to see how the interconnects that are used to communicate with these devices need to be designed and how their design would impact performance and overall size.

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