Performance Analysis of Double Gate Junctionless Tunnel Field Effect Transistor: RF Stability Perspective

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***Abstract*—This paper investigates the RF Stability performance of the Double Gate Junctionless Tunnel Field Effect Transistor (DGJL-TFET). The impact of the geometrical parameter, material and bias conditions on the key figure of merit (FoM) like Transconductance (g_m), Gate capacitance (C_{gg}) and RF parameters like Stern Stability Factor (K), Critical Frequency (f_k) are investigated. The analytical model provides the relation between f_k and small signal parameters which provide guidelines for optimizing the device parameter. The results show improvement in ON current, g_m, f_t and f_k for the optimized device structure. The optimized device parameters provide guidelines to operate DGJL-TFET for RF applications.**

Keywords*—Junctionless tunnel FET; band to band tunnelling; High-k; RF stability; critical frequency

I. INTRODUCTION

For the past four decades, the semiconductor industry is supplemented with CMOS devices due to the continuous growth of Semiconductor Technology. During this regime, the silicon device physical dimensions were reduced to nanometre domain and further scaling (Tens of Nanometre) is limited by Short Channel Effects (SCE) posed by CMOS devices [1-6]. To overcome such challenges, Multi-gate devices are proposed, which shown excellent immunity to SCE and yielded better scalable operations [7-9]. Beyond 30nm, these Multi-gate devices also suffer SCE's and to overcome them, Tunnel Field Effect Transistor (TFET) is proposed which has gained wider significance because of its low subthreshold slope and small leakage current [1-2, 10-14]. Moreover, the tunnel FET device suffers from low ON current and requires abrupt junctions for tunnelling [15]. To overcome the fabrication challenges posed by the MOS and TFET devices, a new transistor called Junctionless transistor (JL) with no doping gradients is proposed to achieve good ON and OFF states [16-17]. Even though the JL device has better scalable performance than the MOSFETs, still it suffers from the low subthreshold slope. To counter the above challenges, Junctionless Tunnel Field Effect Transistor (JL-TFET) is proposed, which exhibits better subthreshold slope of 24mV/decade and DIBL of 38mV/V as compared to conventional JLFET [18-19]. Further, most of the research is carried on investigating the analog performance metrics like Transconductance (gm), unity gain cut off frequency (fT), output conductance (gd) and Intrinsic gain (gm/gd) for the n-type and P-type Double Gate junction and Junctionless TFET [20-21]. Impact of geometrical variability's on the performance of JLTFET and Junctionless hetero structure TFETs (HJLTEFT) is investigated and proposed pocket oxide narrower source side HJTFETs (PNS-HJTFETs) for better performance [22]. The effect of the gate dual material (DMG) and gate engineering approach on the performance of DGJL-TFET is studied [23-25]. Comprehensive analysis on the 20nm HJLTFETs with high-k gate oxide material is presented [26]. The authors have investigated the influence of spacer on ION/IOFF ratio and gm of a DG JLTFET [27]. Impact of dual k spacer on the digital and analogue performances of JL TFET, formed with different substrates is analyzed [28-29]. Influence of parameter fluctuations caused by process variations on the RF stability of Double Gate Tunnel FET (DG-TFET) is reported by k.sivasankaran.et.al [30]. Influence of high-k material on the RF stability performance of Double Gate Junctionless FET is studied [31] and proposed an optimized structure for the better RF performance [32]. The impact of the high-k gate dielectric and dual spacer on the RF stability Performance of JLTFETs is not been studied before. Most of the studies [18-27] focused on analyzing the behaviour of JL-TFETs with and without high-k materials for improving the DC and analogue performance but not on the stability aspects of the device.

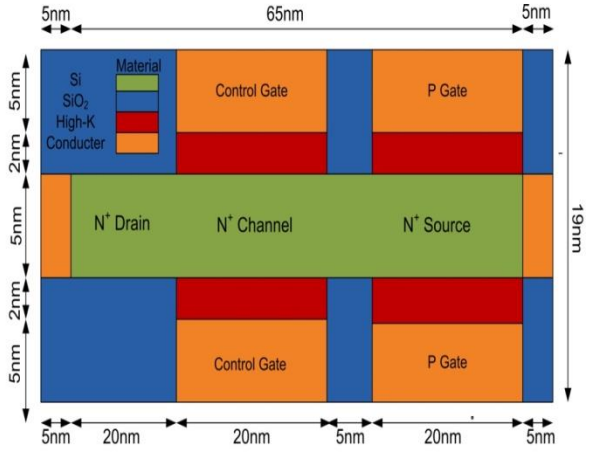

Fig. 1. Schematic Representation of DGJL-TFET Considered for Simulation.

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In this work, we have evaluated the RF Stability performance of the DGJL-TFET for different gate oxide materials and different isolation spacers. Further, the effect of geometrical variations towards the critical frequency is also analyzed for proposing the optimized device.

The remainder of the paper is organized as follows: Section 2 describes the DGJL-TFET considered for simulation. Section 3 gives the device Calibration and DC characteristics. RF Stability performance of the DGJL-TFET for different gate oxide materials is presented in Section 4. The results are discussed in Section 5. The optimized device structure is proposed in Section 6. Finally, the conclusion of the work is presented in Section 7.

II. Device Structure and Simulation

Fig. 1 shows the schematic of the DGJL-TFET. The device is heavily n-type doped 20nm long Si-channel with Source/Drain extension of 20nm [18]. The gate oxide thickness (t_{ox}) is 2nm and device doping profile is maintained at $1x10^{19}$ cm^{-3} for silicon body thickness of 5nm. The device is operated with two gates with different work functions: one gate called control-gate (CG) which is used to control the charge flow in the channel (ON and OFF of the device) by sweeping a control-gate voltage (V_{CG}) from 0V to V_{DD} and another one is P-gate (PG), used to convert the N^+ source of DGJL-TFET to P-type by using gate work function engineering for tunnelling operation. The spacer width, which isolates the CG and PG of the device, is 5nm. All the simulations are performed using a 5.15.32.R version of Silvaco Atlas [33]. A non-local band to band (BTBT) tunnelling model is used to estimate the TFET device performance [18] by considering the tunnelling along the lateral direction between source and drain. Due to heavy doping of the channel, the band gap narrowing (BGN) model is considered and because of the high impurity atom present in the channel, the Shockley-Read-Hall (SRH) recombination model is enabled. Both quantum confinement effect, as well as interface trap effects in TFETs on the non-local band to band tunnelling, are considered by including quantum confinement (QC) model developed by Hansch [33][34] and Schenk [33][35] trap-assisted tunnelling (TAT) model. The work function of Control Gate is taken as 4.3eV for switching the layer under it as intrinsic and platinum metal [36] with a work function of 5.93eV is considered for P-Gate to make the layer under it as P-type region.

III. Device Calibration

A. DC Characteristics

Fig. 2(a) shows the OFF-state charge carrier concentration profile of DGJL-TFET (Drain Source Voltage, V_{DS}=1V and Control Gate Source Voltage, V_{CGS}=0). From Fig. 2(a) it is evident that the device is behaving like N^+-I-P^+ device. Energy band profile of DGJL-TFET in OFF state is presented in Fig. 2(b). The energy gap between the valence band and conduction band is large, due to which tunneling probability of charge carriers through the tunneling region is negligible. Hence, the current flowing in the off sate is small and is only due to the leakage current flowing in N^+-I-P^+ diode.

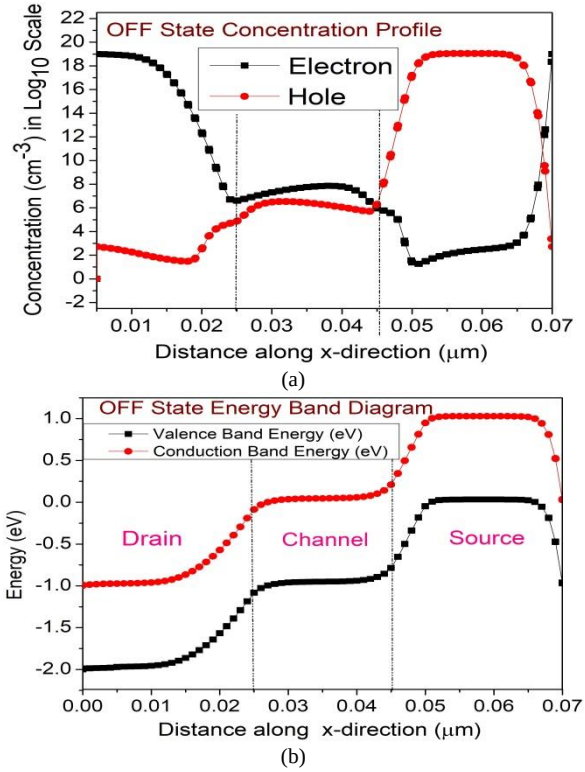


Fig. 2. (a) Electron and Hole Concentration of DGJL-TFET in OFF-State. (b) OFF State Energy Band Profile of DGJL-TFET.

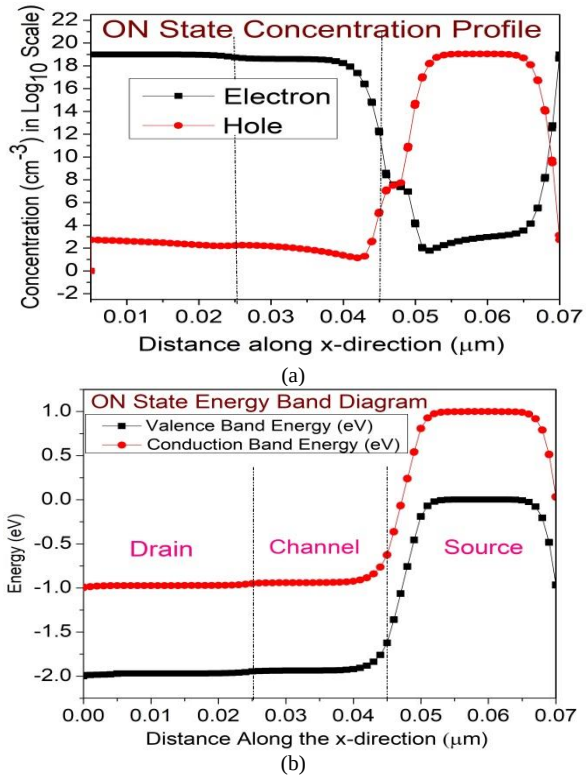


Fig. 3. (a) Electron and Hole Concentration of DGJL-TFET in ON-State (b) ON State Energy Band Profile of DGJL-TFET.

Fig. 3(a) shows the ON state (V_{DS} = 1V, V_{CGS} = 1V) charge concentration profile of DGJL-TFET. By looking at Fig. 3(a), it is evident that when a voltage of 1V applied between CG and source, the layer beneath the CG is converted to N^+, due to which electron concentration in the channel is increased. The rise in electron concentration is due to the increase of tunneling probability of the charge carriers moving from the source to channel. The energy band profile of DGJL-TFET in ON-state is shown in Fig. 3(b), it clearly shows that the narrow bandgap present between the channel and source, due to which tunneling width (λ) is small, subsequently the tunneling probability of the electrons flowing from source to channel is increased and thereby increasing the device ON current.

It is reported that for TFET devices, ON current can greatly improve with the use of high-k materials as gate dielectric [24]. So high k materials like TiO_2 (ε_r=80), HfO_2 (ε_r=25) and Al_2O_3 (ε_r=9) as gate dielectrics [18] are considered for studying their impact on stability of the device with a fixed physical thickness of 2nm.

B. Transfer Characteristics

The transfer characteristics of DGJL-TFET (depicted in Fig. 1) for various gate dielectric materials are shown in Fig. 4. It is observed that the gate oxide with high-k material gives higher ON current and improved subthreshold swing. The improvement in ON current with high-k gate dielectrics mainly due to the reduction of tunneling width (λ), in return, increases the nonlocal tunneling probability according to the WKB approximation, given by equation 1 and also due to the increase of gate coupling with the channel. From Fig. 4, it is observed that the ON current of 34.5μA/μm for a TiO_2 gate dielectric and 0.295μA/μm for Al_2O_3 gate dielectric, with both V_{CGS} and V_{DS} are at 1V.

$$T_t = \exp\left(-\frac{4}{3}\frac{\lambda\sqrt{2m^*}}{3qh(E_g+\nabla\phi)}(E_g)^{3/2}\right) \quad (1)$$

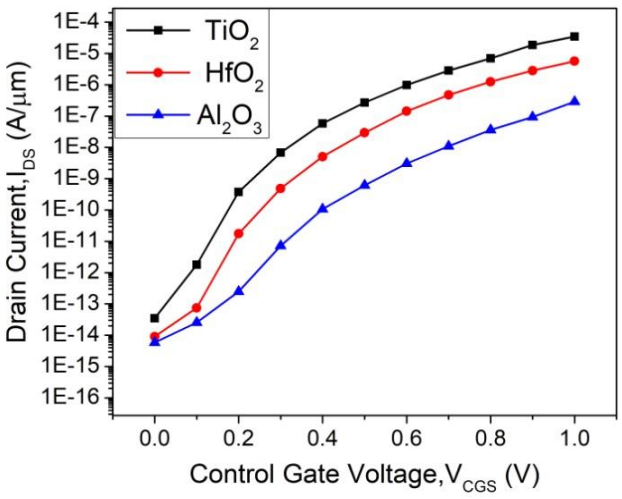


Fig. 4. Transfer Characteristics of DGJL-TFET for Various Gate Dielectric Material Ranging from k= 9 to k=80 with V_{CGS} Sweeping from 0 to 1V and V_{DS} at 1V.

IV. RF Stability Performance of DGJL-TFET

An important phase in the overall analysis of transistor is to identify its potential stability. This may be achieved by calculating the Stern stability factor (K), which specifies the device is unconditionally stable or conditionally stable [37-39]. If K value is greater than one, then the transistor is unconditionally stable, otherwise, it is conditionally stable and which leads to oscillations at some frequency. Equation 2 given by P.Stern in terms of Y parameters is used to calculate the K value of a transistor.

$$K = \frac{2\,\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \quad (2)$$

Where Y_{11} and Y_{22} are admittances, Y_{12} and Y_{21} are known as transfer admittance of a two port network.

$$Y_{11} = \omega^2\left(R_{gs}C_{gs}^2 + R_{gd}C_{gd}^2\right) + j\omega(C_{gs}+C_{gd}) \quad (3)$$

$$Y_{12} = -\omega^2 R_{gd}C_{gd}^2 - j\omega C_{gd} \quad (4)$$

$$Y_{21} = g_{mi} - \omega^2 R_{gd}C_{gd}^2 - j\omega C_{gd} + \tau g_{mi} \quad (5)$$

$$Y_{22} = -g_{dsi} + j\omega(C_{gs}+C_{gd}) + \omega^2 R_{gd}C_{gd}^2 \quad (6)$$

Substituting equations 3 to 6 in equation 2 will further simplify the K, which is given by equation 7.

$$K \cong \frac{\omega(R_{gs}g_{ds}C_{gg}^2 + 2R_{g_d}g_mC_{gg}C_{gd} + C_{gg}^2)}{C_{gd}\sqrt{2\omega^2 g_m C_{gg}^2 + g_m^2}} \quad (7)$$

Critical frequency (f_k) is one of the key RF performance parameter, specifies at what frequency device attains unconditionally stability. By substituting the K=1 in Equation 7 along with some approximations is simplified to equation 8 which is used to calculate the f_k of the device in terms of various parameters [40].

$$f_k \cong \frac{f_T N}{\sqrt{g_{ds}g_m R_{gs}M^2 + NM(g_m R_{gd}+1)}} \quad (8)$$

where, f_T is the Unity-gain cut-off frequency, which is one of important metric of analog characteristics of the device, specifies the frequency at which the current gain reaches to unity and is expressed as

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (9)$$

$$M = \frac{C_{gs}}{C_{gg}} \quad (10)$$

$$N = \frac{C_{gd}}{C_{gg}} \quad (11)$$

$$Cgs = Cgsi + Cfext + Cfin \quad (12)$$

$$Cgd = Cgdi + Cfext + Cfint \quad (13)$$

The other parameters mentioned in equation 8 are output-conductance (g_{ds}), gate-source resistance (R_{gs}), gate-drain resistance (R_{gd}), gate-capacitance (C_{gg}), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) without taking into account of overlap capacitance [39]. The internal fringing field (C_{fint}) as well as external fringing field (C_{fext}) is expressed as:

$$C_{f\,int} = [\frac{W\varepsilon_{si}}{3\Pi}\ln(1+\frac{t_{si}}{2t_{ox}}\sin(\frac{\Pi}{2}\frac{\varepsilon_{ox}}{\varepsilon_{si}}))]e^{-(\frac{(V_{gs}-V_{FB}-2\phi_f-V_{ds})}{(3/2)\phi_f})^2} \quad (14)$$

$$C_{fext} = [\frac{2W\varepsilon_{ox}}{3\Pi}\ln(1+\frac{t_g}{2t_{ox}})] \quad (15)$$

ε_{ox} and ε_{si} are dielectric constants of gate oxide and silicon materials. Where W, t_{si}, t_{ox} and t_g are width, silicon thickness, oxide thickness and gate material thickness, respectively. Φ_f and V_{FB} are Fermi potential and flat band voltage, respectively.

The stability factor is evaluated using equation 7 for DGJL-TFET with various gate oxide materials, whose dielectric values range from 9 to 80 is shown in Fig. 5. From the results, we can observe that the DGJL-TFET with a low-k gate oxide material (k=9) is attaining unconditional stable at a lower frequency at 6 GHz than the high-k gate dielectric (k=80) at a frequency of 130 GHz. Lower f_k value is exhibited by low-k gate dielectrics is mainly due to low ON current, low gate capacitance and smaller gain associated with it.

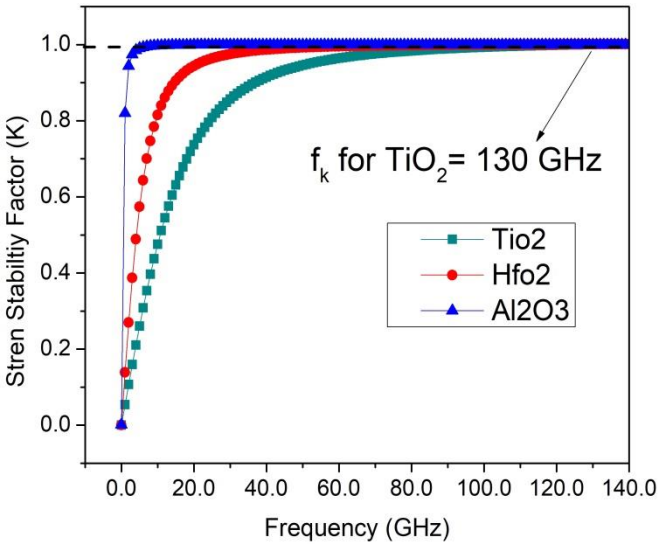


Fig. 5. Stern Stability Factor (K) of the DGJL-TFET Device for Various Gate Oxide Materials.

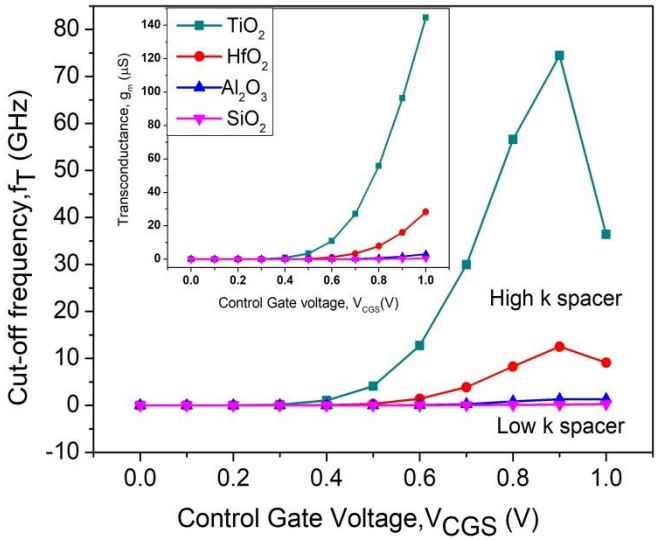
V. Results and Discussion

A. Impact of Gate Dielectric Material (k) on Critical Frequency (f_k)

Fig. 6(a) shows the gate dielectric material influence on the cut off frequency (f_T) and transconductance (g_m).

Fig. 6(a) inset, it is observed that g_m is increasing with increase of dielectric constant of gate oxide material. As with the increase of gate dielectric constant, the tunneling width reduces due to which the tunneling probability increases, thereby enhancing the I_{ON} and thereby g_m. Because of the increase of relative permittivity of the gate oxide material with the rise of the gate dielectric constant, the C_{gg} also increases. Due to higher impact of g_m over the C_{gg}, f_T which is calculated from simulation values g_m and C_{gg} using equation 9 is increasing with increase in gate dielectric value.

As discussed earlier, from Fig. 6(a), due to improved performance of f_T, C_{gg} and g_m with a high-k gate dielectric, DGJL-TFET with high-k gate material (HfO_2, TiO_2) yielded higher f_k as compared to low-k gate material (SiO_2). From Fig. 6(b) f_k which is calculated using equation 8 is 1.5GHz for low-k gate oxide material (SiO_2) and for 130GHz for high-k gate oxide material (TiO_2). Various parameters which has effect on the stability and f_k for various oxide materials are presented in Table I.



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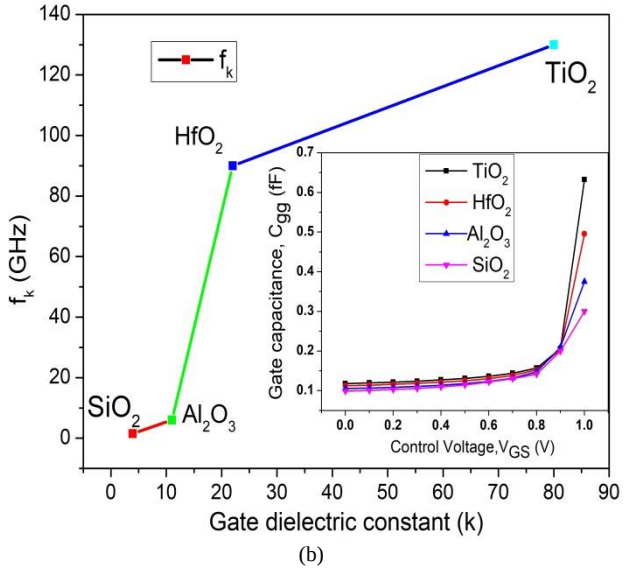


(b)

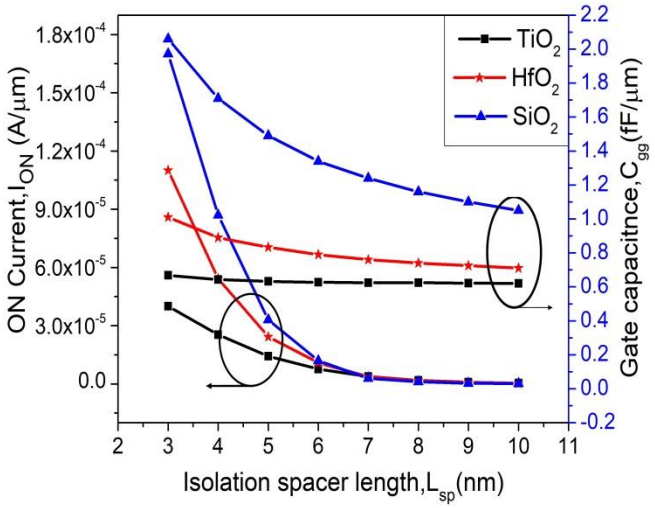
Fig. 6. Variation of (a) f_T and g_m (Inset) with Control Gate Voltage (V_{CGS}) and (b) f_k as Function of Gate Dielectric Constant (k).

TABLE. I. KEY PERFORMANCE METRICS OF DGJL-TFET FOR DIFFERENT GATE OXIDES AT VCGS= VDS=1V

Gate oxide material	I_{on} (μA/μm)	g_m (μS)	C_{gg} (fF)	f_T (GHz)	f_k (GHz)
SiO_2	0.1	0.5	0.269	0.2	1.5
Al_2O_3	0.5	3.09	0.375	1.31	6
HfO_2	5.71	28.4	0.495	12.5	90
TiO_2	34.9	145	0.633	74.7	130

B. Impact of Isolation Spacer Length (L_{sp}) on f_k

In the previous subsection, it is observed that the ON current of the DGJL-TFET is improved with the aid of high-k gate dielectrics. The other way to increase I_{ON} is by scaling the isolation spacer length (L_{sp}), with the aid of charge plasma concept [24]. With scaling of spacer length (L_{sp}), the gate controllability over the source-channel region is increased, which reduces the tunneling barrier height, due to which the tunneling probability increases, subsequently increasing the I_{ON}. However, this improved I_{ON} is obtained at the expense of increased C_{gg}, which is shown in Fig. 7(a).



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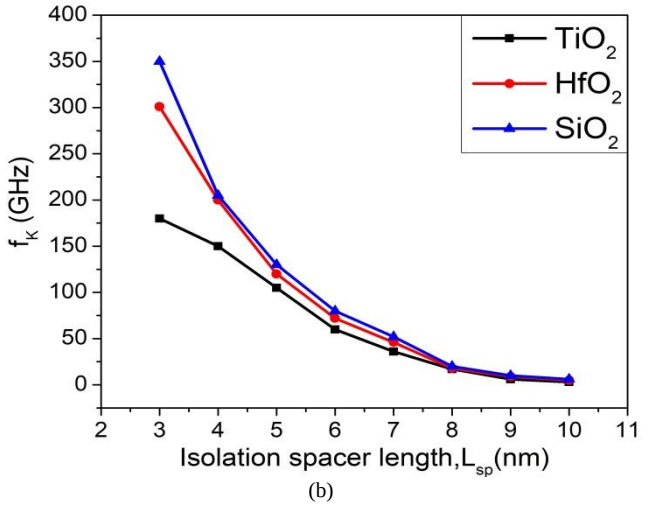


(b)

Fig. 7. Variation of (a) I_{ON} and C_{gg} and (b) f_k as Function oF isolation Spacer Length of DGJL-TFET.

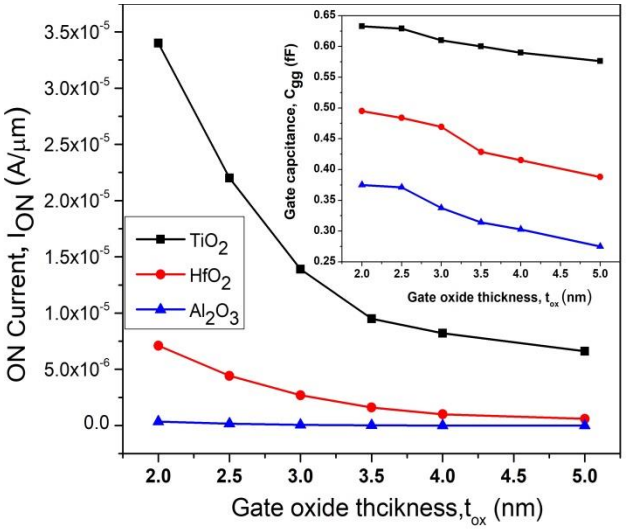
Fig. 7(b) shows the f_k variation with the scaling of isolation spacer (L_{sp}) of DGJL-TFET for different spacer material with 2nm TiO_2 as a gate dielectric. It is evident from Fig. 7(b) that, f_k is increasing with the scaling of the L_{sp}. While scaling the L_{sp} from 10nm to 5nm, the impact of it on f_k is not as much of for all the spacer materials, but further scaling of L_{sp} below 5nm the impact is large. This impact is largely attributed by interface defects at high-k oxide and Si interface, the induced trapped charges and capacitive fringing field's associated with high-k spacers. For TiO_2 spacer, f_k is varied from 3GHz to180GHz when L_{sp} scaled from 10nm to 3nm. However, a large variation of f_k nearly twice as that of the high-k spacer (TiO_2) is noticed with the low-k spacer (SiO_2). i.e., f_k is varied from 6 GHz to 350 GHz, when L_{sp} scaled from 10nm to 3nm.

C. Impact of Gate Oxide Thickness (t_{ox}) on f_k

Tunneling process in T-FET devices is greatly affected by the variation gate oxide thickness (t_{ox}), this effect is noticed due to the variation of gate-capacitive coupling with variation of t_{ox}. As per WKB approximation, oxide thickness affects the tunneling probability by modulating the tunneling width. Equation 16 gives the dependency of tunneling width in terms of gate oxide thickness and other parameters. A thinner gate oxide will have less tunneling width (λ) and vice versa for thicker gate oxides.

$$\lambda = \sqrt{\left(\frac{t_{ox} t_{si} \varepsilon_{si}}{\varepsilon_{ox}}\right)} \quad (16)$$

The ON current of device with t_{ox}=5nm is smaller when compared to 2nm t_{ox} device, since 5nm oxide thickness devices have low capacitive coupling, due to which it has a lesser influence on the tunneling phenomena. Through simulation, it is also observed that irrespective of gate oxide material, DGJL-TFET exhibits improved I_{ON} with the scaling of the $t_{ox.}$ It is also observed that TiO_2 gate dielectric with t_{ox} =5nm has better I_{ON} (6.6 μA) than low-k gate dielectric (Al_2O_3) with t_{ox}= 2nm (0.35 μA) The simulated values effecting the stability and f_k with t_{ox} scaling for TiO_2 gate oxide material are given in Table II. Fig. 8(b) shows f_k variation with the scaling of t_{ox} for different gate oxide materials of a DGJL-TFET with 5nm SiO_2 isolation spacer. It is observed that, with the scaling of t_{ox}, DGJL-TFET with low-k gate dielectric has lower f_k then that of high-k gate dielectric. The simulation results illustrate that f_k for TiO_2 is varied from 68 GHz to 130 GHz and 0.2GHz to 6GHz for the Al_2O_3 with the scaling of t_{ox}. When t_{ox} scaled from 5nm to 2nm, nearly 50% increase in f_k for TiO_2 material is noticed and it is because of the large variations in I_{ON}, g_m, and C_{gg} with the scaling of t_{ox}. Fig. 9(a) illustrates a comparative impact of drain side spacer materials on the stability of the DGJL-TFET with 2nm TiO_2 as gate oxide and 5nm SiO_2 as isolation spacer and at an L_{dsp} of 15nm. It is observed that, drain spacer material has smaller impact on stability factor and almost same for all the spacers. As the drain spacer does not have tendency to affect the tunneling width, the current of the device and other stability parameters are virtually the same.



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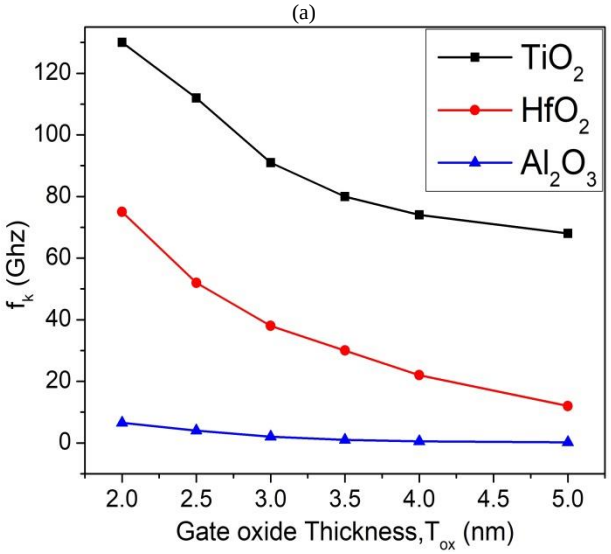


(b)

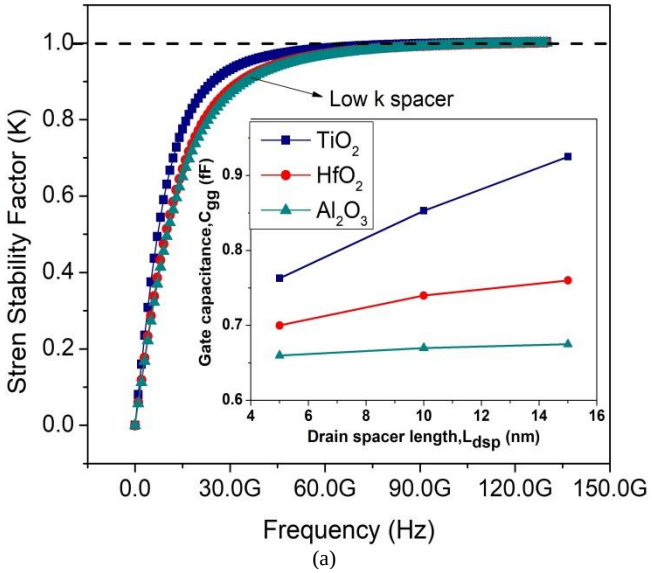
Fig. 8. Variation of (a) ON Current and C_{gg} and (b) Critical Frequency (f_k) with Respect to Scaling of Gate Oxide Thickness (t_{ox}) for different Gate Oxide Material of DGJL-TFET with 5nm SiO_2 as Isolation Spacer.

TABLE. II. KEY PERFORMANCE METRIC VALUES WITH THE SCALING OF TiO_2 GATE OXIDE OF DGJL-TFET

Gate oxide material=TiO_2	I_{on} (μA/μm)	g_m (μS)	C_{gg} (fF)	f_t (GHz)	f_k (GHz)
2 nm	34.9	145.0	0.63	74.4	130
2.5 nm	19.2	84.5	0.62	41.1	112
3 nm	14.0	64.4	0.61	28.9	91
3.5 nm	9.54	47.3	0.60	15.40	80
4 nm	8.27	38.1	0.59	11.8	74
5 nm	7.45	35.1	0.57	9.52	68

D. Impact of Drain Side Spacer and Drain Spacer Length (L_{dsp}) on f_k

From the Fig. 9(b), as L_{dsp} is scaled from 15nm to 5nm, f_k is increasing marginally for all the spacer materials and it is mainly because of the reduction spacer fringing fields and the capacitive area, thereby reducing the gate capacitance which is shown in the inset of Fig. 9(a). With the L_{dsp} scaling, C_{gg} is reduced largely for high k spacer and slightly varied for low k spacer. The parameters related to equation 3, like I_{ON}, g_m, f_t, are almost constant with spacer material and spacer length but the variation in C_{gg}, which is large for high k spacer is only impacting the f_k. Therefore f_k for TiO_2 spacer varied nearly 20 GHz, when L_{dsp} is scaled from 15 nm to 5nm.



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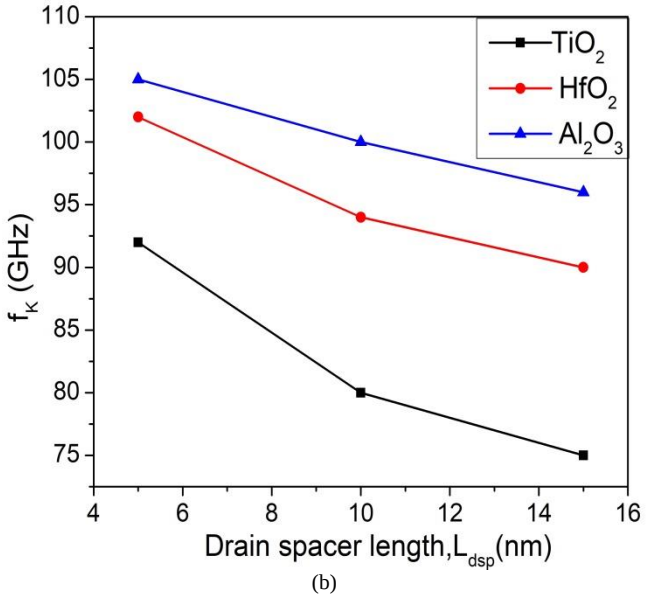
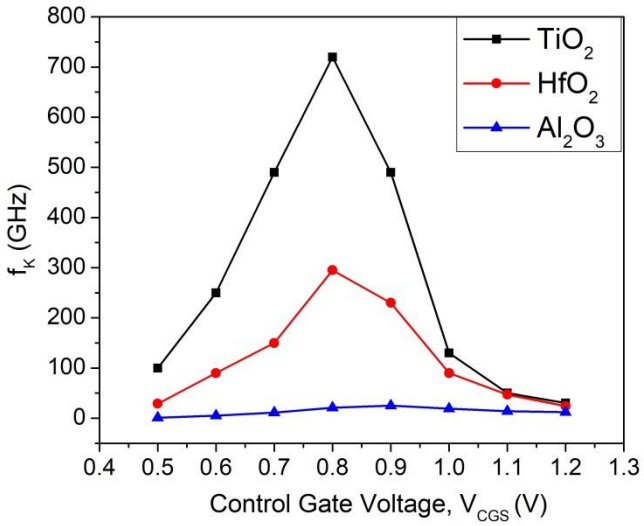


(b)

Fig. 9. (a) Stability Factor (K) Variation with Frequency for L_{dsp} 15nm and (b). f_k Variation with Scaling of L_{dsp} of a DGJL-TFET for different Spacer Materials.

E. Impact of Gate and Drain Bias on f_k

Fig. 10(a) shows the impact of control-gate voltage (V_{CGS}) on the f_k for 5nm isolation spacer DGJL-TFET for different gate oxides at V_{DS} of 1V. As gate bias V_{CGS} varied from 0.4V to 0.8V, f_k is increased for all gate oxides. since the device current, g_m and C_{gg} asscoiated with high- k gate oxide materials is large. Therfore the f_k of TiO_2 material is increased at a much higher rate than that of Al_2O_3 material. At higher gate bias, i.e., when V_{CGS} is increased beyond0.8V, f_k for Al_2O_3 lies in the same order but for HfO_2 and TiO_2 material it decreases to a larger extent. The decreasing in f_k for TiO_2 material is due to the large varition in C_{gg} and smaller variations in I_{ON} and g_m with control gate bias beyond 0.8V. The lowest value of f_k for TiO_2 material is 25 GHz at gate voltage of 1.2V. Finally, it is noticed that higher the control-gate voltage, lower the f_k value.



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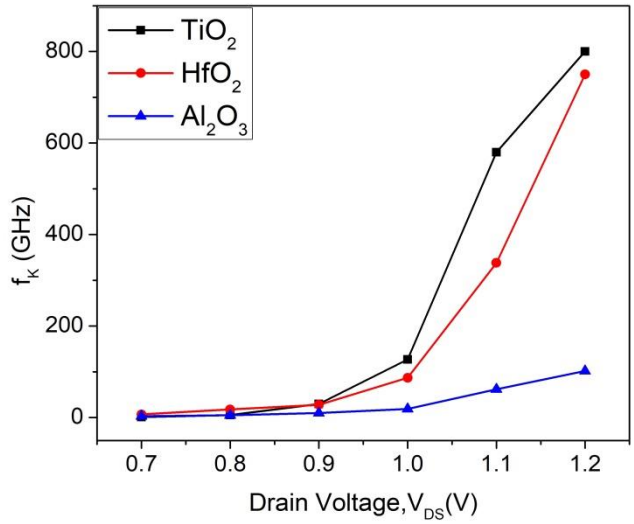

(b)

Fig. 10. Variation of f_k with (a) Control Gate Voltage and (b) Drain Voltage.

Fig. 10(b) shows f_k variation with respect to drain bias scaling for different gate oxide materials of DGJL-TFET with 5nm as isolation spacer. As drain voltage V_{DS} changing from 0.7V to 0.9V, f_k is of the same order and the insignificant difference is noticed for all the gate oxide. But for V_{DS} above 0.9V, the f_k of high-k gate dielectric (TiO_2) is much higher when compared to low-k gate dielectric (Al_2O_3). This is attributed by the decrease of output conductance (g_{ds}) and an increase of I_{ON} with the increase of drain voltage for TiO_2 gate oxide material. So, higher drain bias and high-k gate oxide material will yield higher f_k and vice versa.

VI. RF Performance of Optimized DGJL-TFET

The device geometry parameters like gate oxide thickness, spacer material, spacer length, gate dielectric material, and supply voltages are identified from the preceding sections for the optimization of the device for better RF stability performance is shown in Fig. 11. From the preceding section results, TiO_2 material is taken as gate dielectric material for the optimized DGJL-TFET structure with t_{ox} of 2nm. TiO_2 material is chosen as drain spacer and isolation spacer of a length 15nm and 3nm respectively. The structure is simulated with supply voltages at V_{CGS}=1.2V and V_{DS}=0.8V.

Fig. 12 shows the stern stability factor (K) for the optimized structure. The device attaining stability at a lower frequency and yielding lower f_k of 17.5GHz without degrading the I_{ON}. The low value of f_k is due to larger capacitance and larger fringing fields associated with TiO_2 gate oxide material. Since the optimized device exhibiting lower f_k, hence at a lower frequency,the device becomes unconditionally stable thereby making it a best suitable device for high frequency applications.

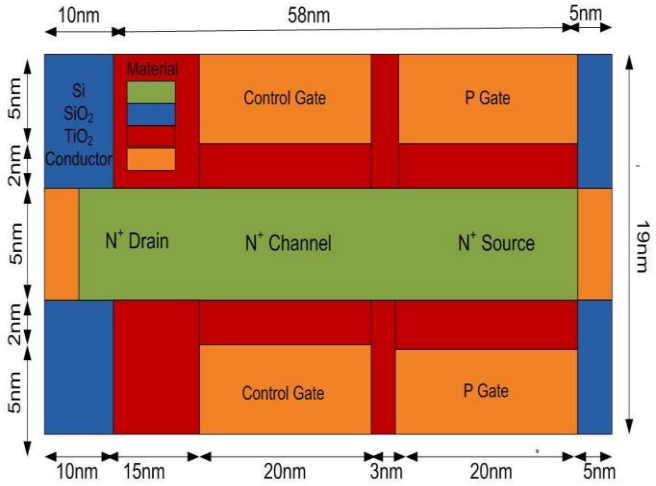

Fig. 11. Optimized DGJL-TFET with TiO_2 as Gate Oxide.

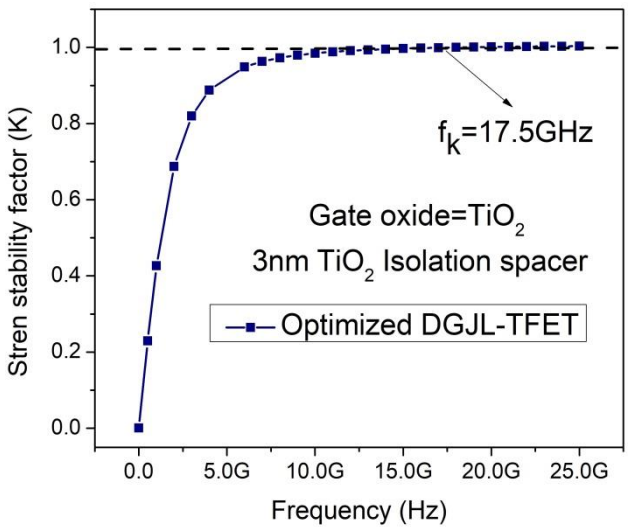

Fig. 12. Stern Stability Factor (K) as a Function of Frequency for optimized DGJL-TFET.

VII. Conclusion

In this paper, we have investigated the influence of high-k gate dielectrics / high-k spacer on the RF stability performance of 20nm channel DGJL-TFET. From the simulation results, it is observed that the device with low-k gate dielectric attains stable at lower frequencies, but yielding low ON current. It is also noticed that high-k as an isolation spacer is responsible for the obtaining lower f_k. In addition, the effect of geometrical variability's towards f_k is studied and results showed decreasing trend with the increase of the spacer length, gate oxide thickness, but an increased trend for drain voltage. Finally, the optimized structure is proposed for yielding the better stability and lower f_k, by which we can avoid the additional circuit. The proposed DGJL-TFET exhibits f_k of 17.5GHz. In summary the DG-JTFET is promising device, suitable for low power and analog/RF applications.

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