Hybrid Concatenated LDPC Codes with LTE Modulation Schemes

Mohanad Alfiras[1]
Communication and networks Engineering, Gulf University, Manama, Kingdom of Bahrain

Wael A. H. Hadi[2], Amjad Ali Jassim[3]
Communication Engineering Department
Engineering college, Al-Technology University
Baghdad, Iraq

***Abstract*—In a communication system, the LDPC code is considered as a good performance error correcting code which reaches near Shannon limit. In this paper a hybrid LDPC code is proposed, the hybrid term here refers to the serial concatenation of parallel LDPC codes group and a single serial LDPC code. The outer two parallel LDPC codes encoder represents outer encoder where the single LDPC encoder represents the inner encoder. This study also emphases on the performance of a hybrid coding system in consideration with three modulation schemes. The modulation schemes include quadrature phase shift keying (QPSK) and two types of quadrature amplitude modulation; 16-QAM and 64-QAM. These modulation schemes are selected due to their importance in modern communication applications, such as long term evolution (LTE); such schemes are the standard modulation schemes used with LTE system. This study investigates different LDPC code rates such as 1/2 and 1/3 and simulates the AWGN communication channel using MATLAB. The simulation results show improvement in bit error rate (BER) when using 1/3 LDPC code rate in the designed system rather than 1/2, but it also increases the system complexity. In the end, all simulation results, the comparison between different cases of LDPC code rates and system performance are summarized.**

***Keywords*—Coding; modulation; Hybrid; concatenation; low density parity check**

I. Introduction

G. David Forny introduced the concept of concatenated codes in 1965 as a method to improve system code performance [1]. Earlier to this, Gallager in his Ph.D. dissertation at M.I.T invented LDPC codes in 1960 [2]. This paper focuses on the concept that uses the LDPC codes concatenation as an error correction code to improve communication system performance against errors raised during signal transmission through the noisy channel. The code concatenation improves the performance of the error correction code as a group against transmission errors. The simplest form of code concatenation is observed in serial concatenation between two error correction codes. The codes that are involved in serial concatenation can be of different or same type. For example, serial concatenation between two convolutional encoders [3] or between two different error correction codes, such as, read Solomon code and convolutional encoder [4] and between read Solomon code and LDPC code [5]. The error correction code concatenation also has another form which consists of parallel concatenation between two identical error correction codes [6]. For example, the parallel concatenation between two convolutional encoders forms a well-known Turbo code. The concatenation between two parallel convolutional encoders offers the significant BER Turbo code performance, but with increased decoder complexity. The decoder uses complicated algorithms to calculate decoding frame estimation such as SOVA and BCJR algorithms [7]. LDPC codes can be used with the same concept of code concatenation. Therefore, researchers focus on using serial concatenation of LDPC codes of the same code type and rate [8]. In order to form a serially concatenated codes, consider concatenation between LDPC codes of different types as compatible pairs [9]. In order to achieve that, the inner LDPC encoder takes code rates which are fitted in data rate with outer LDPC encoder. This strategy takes benefit of increasing only the inner LDPC encoder size and reduce the system complexity as compared when using two large size LDPC codes. Also, parallel concatenation is applicable for LDPC codes using two identical LDPC codes with a simple modification in the receiver to avoid increasing system decoder complexity [10]. This modification includes taking the sum of the two LDPC decoders that are based on bit flipping algorithm [11]. In many communication applications such as deep space communication systems, there is a need for accurate BER performance against raised communication errors rather than the system complexity [12]. Therefore, the system complexity could be acceptable in some communication applications where the actual goal of the system is to achieve a good BER performance [13]. This work focus on using short length irregular LDPC codes connected in Hybrid form, the term Hybrid concatenation used here refers to two types of concatenated codes, parallel concatenation between two identical LDPC encoders and serially concatenated with inner LDPC encoder. The concatenation strategy should be carefully designed to get better system performance and low system complexity as much as possible. So, different code rates and different modulation schemes are investigated by comparing different system designs.

II. Proposed System Transmitter

The proposed hybrid system transmitter consists of three main stages. First, represented by identical irregular LDPC codes connected in parallel to construct outer encoder. Second, the produced code words from two LDPC encoder are multiplexed to prepare input for the next stage of inner encoder LDPC with length equal to twice individual outer LDPC code. The inner code input frame length will be two times the output of a single LDPC code used to construct the outer parallel

group. Third, the modulation scheme such as QPSK, 16-QAM or 64-QAM considered in modulation stage [14, 15] as LTE standard modulation schemes. The system transmitter is shown in Fig. 1.

In order to process the input data, the Hybrid system transmitter starts by the LDPC1 and LDPC2 encoders which are designed to be identical. Each code of data rate equal to $1/n_1$. There is an interleaver between these parallel LDPC1 and LDPC2 encoders which is denoted by π_1 in Fig. 1. The interleaver rearrange the order of input data frame to construct a new code word which differs from the code word of LDPC1 encoder. The interleaver could be random or another type. Here, the main usage of interleaver is to overcome the effects of burst errors, if found in the received codeword and change it to suppurated errors that could be handled and corrected by LDPC decoder. Each LDPC1 and LDPC2 encoder of code rate

$$k/n_1 = k/n_2 = k/n \quad (1)$$

Where 'k' represents the length of the input data frame, and the 'n' represents the length of the produced code word. Therefore, after the parallel encoding process and multiplexer, it produces a codeword of length

$$1/(2\times n_1) = 1/(2\times n_2) = 1/(2\times n) \quad (2)$$

Inner LDPC encoder is designed to be of different length, not the same as LDPC codes which are used with an outer parallel group. The length of the input data which inner LDPC takes is the same as the length of the produced codeword by the outer parallel group. Then the inner LDPC code rate $1/n_3$, in terms of input is

$$R= (2\times n_1)/(2\times n_1\times n_3) \quad (3)$$

The symbol π_2 in system stands for random interleaver used to enhance system performance against burst errors. In general, for LDPC codes, the larger length LDPC encoder gives the best performance as compared with shorter ones. However, larger LDPC code length means more complex LDPC decoder in system receiver. The inner LDPC3 will be an effective inner encoder, without using a larger encoder.

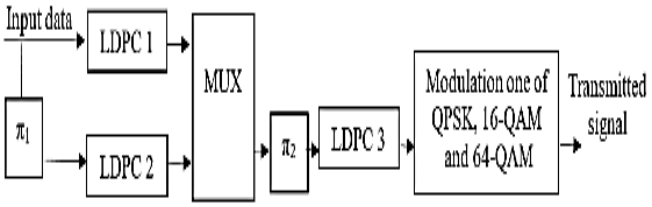

Fig. 1. Hybrid LDPC Code System Transmitter.

III. Proposed System Receiver

The hybrid system receiver starts with the demodulation process which is the same as the modulation scheme used in the system transmitter. The decoding process starts in reciprocal order of the transmitter encoder process. It starts by decoding LDPC3 which represent inner encoder of the transmitter. This decoder uses the LLR (Log Likelihood Ratio algorithm) [16]. The LDPC decoder gives estimation output which is denoted by $\hat{E}_3$. The decoding algorithm LLR is described as follow [16]:

The input to the LDPC decoder is the log-likelihood ratio (LLR), $L(c_i)$, which is defined by

$$L(c_i) = log\left(\frac{\Pr(c_i=0|\ channel\ output\ for\ ci)}{\Pr(c_i=1|channel\ output\ for\ ci)}\right) \quad (4)$$

Where c_i is an ith bit of the transmitted codeword c. There are three key variables in the algorithm: $L(r_{ji})$, $L(q_{ij})$, and $L(Q_i)$. $L(q_{ij})$ is initialized as $L(q_{ij}) = L(c_i)$. For each iteration, update $L(r_{ji})$, $L(q_{ij})$, and $L(Q_i)$ using the following set of equations [16]:

$$L(r_{ji}) = 2\ \text{atanh}(\prod_{i'\in V_{j\backslash i}} \tanh(\tfrac{1}{2}\ L(q_{i'j})))$$

$$L(q_{ij}) = L(c_i) + \sum_{j'\in c_i\backslash j} L(r_{j'i})$$

$$L(Q_i) = L(c_i) + \sum_{j'\in c_i} L(r_{j'i}) \quad (5)$$

$\hat{E}3$ represents the estimated output from $LDPC_3$, which is passed to de-multiplexer to redirect $\hat{E}_3$ into two groups which are inputs for LDPC decoder one and LDPC decoder two, respectively. The LDPC decoders of one and two use the same described decoding algorithm LLR. Such a process at the end produce another two estimations denoted by $\hat{E}_1$ and $\hat{E}_2$ refers to each decoder of the parallel group. The two estimations then summed before the decision. The decision represents the final receiver stage to produce received data. Fig. 2 shows the proposed system receiver.

Where the symbol π^{-1} refers to random de-interleaver.

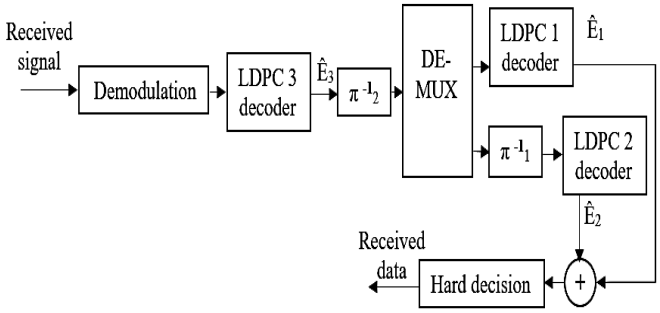

Fig. 2. Proposed Hybrid System Receiver.

IV. Simulation Parameters

The simulation includes the generation of two sets of irregular LDPC codes. First of rate 1/2 and second of rate 1/3. Table I and Table II summarize the description where the code is described by C_b (N, K), N codeword length, and K input data length.

The simulation takes in consideration of multiple hybrid system designs; it discusses the increase in the length of generated irregular LDPC codes and also designs the hybrid system with two LDPC code rates, first represented by rate 1/2 and the second of rate 1/3. It gives us more sense about increasing LDPC code rate and length and its effect in system BER performance.

TABLE I. LDPC CODES RATE 1/2

Design	Outer encoder parallel group		Inner encoder
	LDPC1	LDPC2	LDPC3
Case 1	C_b (48, 24)	C_b (48, 24)	C_b (192, 96)
Case 2	C_b (96, 48)	C_b (96, 48)	C_b (384, 192)
Case 3	C_b (144, 72)	C_b (144, 72)	C_b (576, 288)
Case 4	C_b (192, 96)	C_b (192, 96)	C_b (768, 384)
Case 5	C_b (240, 120)	C_b (240, 120)	C_b (960, 480)

TABLE II. LDPC CODES RATE 1/3

Design	Outer encoder parallel group		Inner encoder
	LDPC1	LDPC2	LDPC3
Case 1	C_b (72, 24)	C_b (72, 24)	C_b (432, 144)
Case 2	C_b (144, 48)	C_b (144, 48)	C_b (864, 288)
Case 3	C_b (216, 72)	C_b (216, 72)	C_b (1296, 432)
Case 4	C_b (288, 96)	C_b (288, 96)	C_b (1728, 576)
Case 5	C_b (360, 120)	C_b (360, 120)	C_b (2160, 720)

V. SIMULATION RESULTS

The proposed system simulation includes the cases and their corresponding generated irregular LDPC codes. It splits the system performance as BER vs. SNR into two groups depending on the LDPC code rate. In each case, a modulation scheme is selected from three types of QPSK which are used for low data rate while its symbol consists of two bits; 64-QAM for high data rate with good quality SNR where each symbol consisted of 6 bits and 16-QAM with 4 bits per symbol. These modulation schemes are used as a standard with LTE application [4]. Fig. 3 to 8 shows simulation results, respectively.

The simulation result values (BER) compares different system parameters listed in Table III and Table IV, respectively.

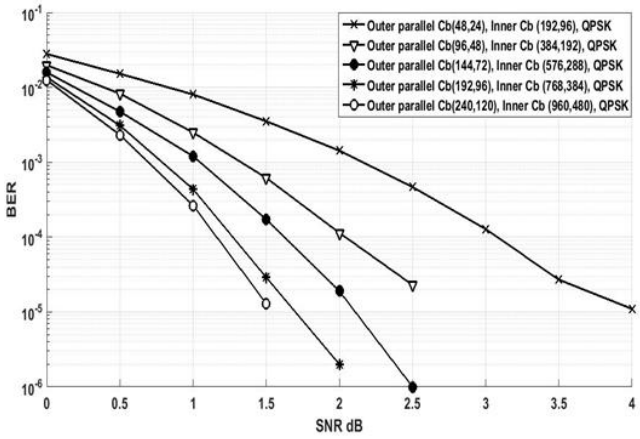

Fig. 3. LDPC Code Rate 1/2, QPSK.

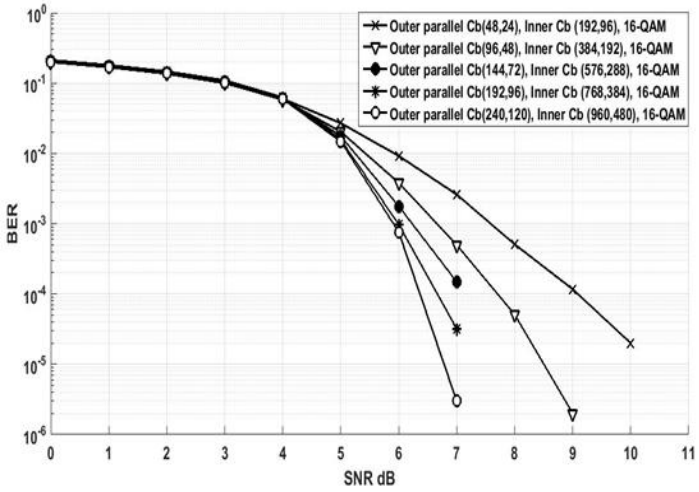

Fig. 4. LDPC Code Rate 1/2, 16-QAM.

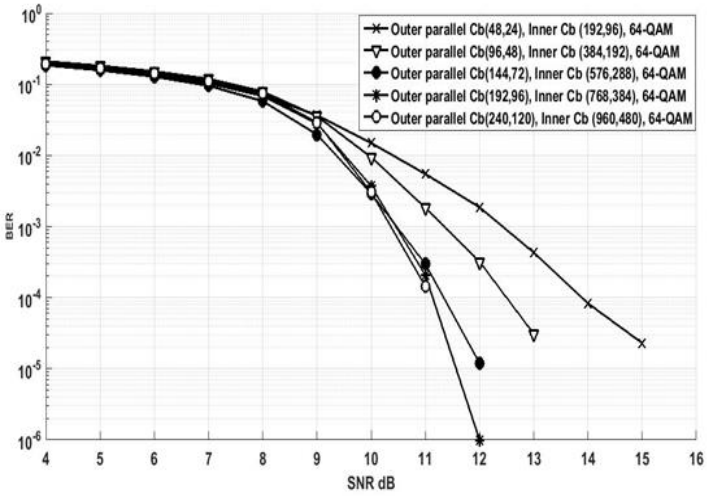

Fig. 5. LDPC Code Rate 1/2, 64-QAM.

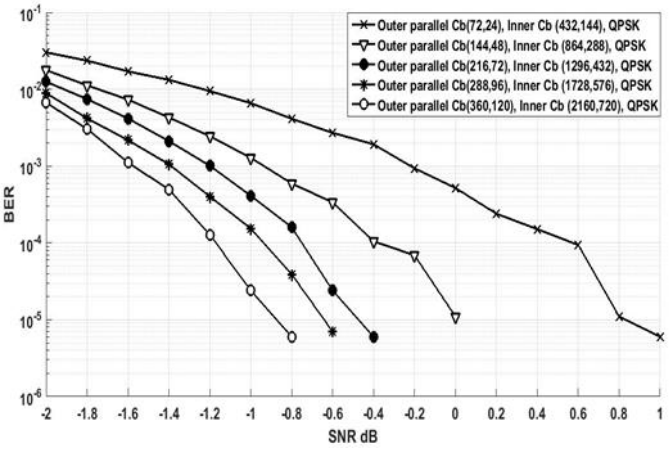

Fig. 6. LDPC Code Rate 1/3, QPSK.

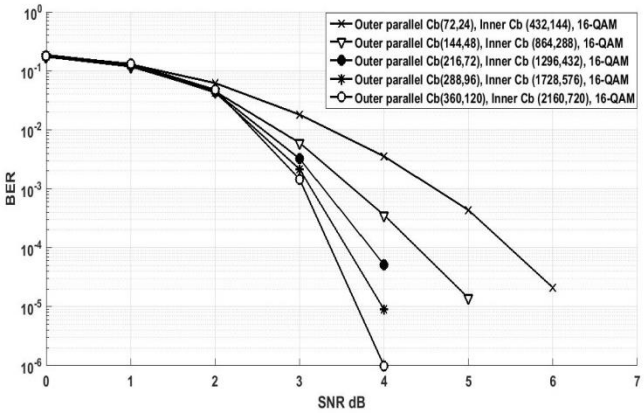

Fig. 7. LDPC Code Rate 1/3, 16-QAM.

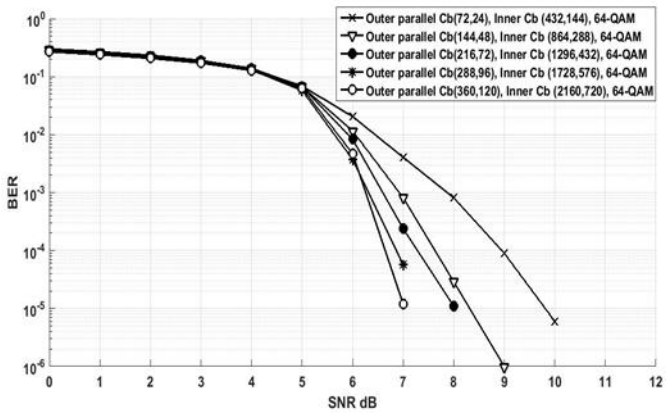

Fig. 8. LDPC Code Rate 1/3, 64-QAM.

TABLE III. SHOWS SIMULATION RESULTS IN COMPARISON TO HYBRID SYSTEM LDPC RATE 1/2

Modulation type	Outer Parallel Two LDPC Codes	Inner LDPC code	SNR	BER
QPSK	Cb(48, 24)	Cb(192, 96)	4	1.1×10^{-5}
	Cb(96, 48)	Cb(384, 192)	2.5	2.2999×10^{-5}
	Cb(144, 72)	Cb(576, 288)	2.5	9.9999×10^{-7}
	Cb(192, 96)	Cb(768, 384)	2	1.9999×10^{-6}
	Cb(240, 120)	Cb(960, 480)	1.5	1.2999×10^{-5}
16-QAM	Cb(48, 24)	Cb(192, 96)	10	2×10^{-5}
	Cb(96, 48)	Cb(384, 192)	9	1.9999×10^{-6}
	Cb(144, 72)	Cb(576, 288)	7	0.000149
	Cb(192, 96)	Cb(768, 384)	7	3.1999×10^{-5}
	Cb(240, 120)	Cb(960, 480)	7	2.9998×10^{-6}
64-QAM	Cb(48, 24)	Cb(192, 96)	15	2.3×10^{-5}
	Cb(96, 48)	Cb(384, 192)	13	3.0999×10^{-5}
	Cb(144, 72)	Cb(576, 288)	12	1.2×10^{-5}
	Cb(192, 96)	Cb(768, 384)	12	9.9997×10^{-7}
	Cb(240, 120)	Cb(960, 480)	11	0.00014399

TABLE IV. SHOWS SIMULATION RESULTS IN COMPARISON TO HYBRID SYSTEM LDPC RATE 1/3

Modulation Type	Outer Parallel Two LDPC Codes	Inner LDPC Codes	SNR	BER
QPSK	Cb(72, 24)	Cb(432, 144)	1	6×10^{-6}
	Cb(144, 48)	Cb(864, 288)	0	1.1×10^{-5}
	Cb(216, 72)	Cb(1296, 432)	-0.4	6×10^{-6}
	Cb(288, 96)	Cb(1728, 576)	-0.6	6.9998×10^{-6}
	Cb(360, 120)	Cb(2160, 720)	-0.8	5.9995×10^{-6}
16-QAM	Cb(72, 24)	Cb(432, 144)	6	2.1×10^{-5}
	Cb(144, 48)	Cb(864, 288)	5	1.4×10^{-5}
	Cb(216, 72)	Cb(1296, 432)	4	5.2×10^{-5}
	Cb(288, 96)	Cb(1728, 576)	4	8.9997×10^{-6}
	Cb(360, 120)	Cb(2160, 720)	4	9.9992×10^{-7}
64-QAM	Cb(72, 24)	Cb(432, 144)	10	6×10^{-6}
	Cb(144, 48)	Cb(864, 288)	9	9.9997×10^{-7}
	Cb(216, 72)	Cb(1296, 432)	8	1.1×10^{-5}
	Cb(288, 96)	Cb(1728, 576)	7	5.6998×10^{-5}
	Cb(360, 120)	Cb(2160, 720)	7	1.1999×10^{-5}

VI. Conclusions

The proposed hybrid system consists of serial concatenation between parallel and serial LDPC codes. The work discusses the different generated irregular LDPC codes. From the simulation, there are two main results; the first result represents the increasing length of LDPC code which shows enhancement in system BER performance as shown in Fig. 3 to 8. The second result is obtained by using LDPC codes of code rate 1/3 instead of rate 1/2 which shows more improvement in system BER performance. This improvement is realized with increased system complexity. However, the designed system is a compromise between cost and performance. Hence, 16-QAM at 7 dB reaches 10^{-5} BER and QPSK -2 dB which shows negative performance. Where 16-QAM reaches 10^{-6} at 4 dB SNR value. The system looks complicated, but it should be noted that the design uses a short length of irregular LDPC codes as maximum C_b (2160, 720) for rate 1/3 LDPC as an inner encoder. The choice between different hybrid systems introduced in this work comes with two considerations, i.e., the performance and system complexity. The proposed hybrid system could be achieved in a practical application using FPGA. Since the LDPC codes show flexibility in the implementation using such technology. The LDPC decoder algorithms provide simple decoding estimation such as Bit Flipping decoding algorithm. Such consideration can reduce the hybrid system complexity.

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