Design Optimization of Power and Area of Two-Stage CMOS Operational Amplifier Utilizing Chaos Grey Wolf Technique

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Abstract—**Low Power Dissipation is an emerging challenge in the current electronics industry. Area shrinking has found the most prominent place and is the foundation of every constricted size in the utilization of CMOS circuits in Integrated Circuit Manufacturing. Functionality in terms of rapidity, dissipation of power, etc. are strongly influenced by the dimensions of transistors in many CMOS Integrated Circuits. The significant formulation parameters in CMOS circuit design to perform optimization of the above-mentioned parameters, and various techniques were projected earlier to a maximum extent possible. Latency, Power, and Dimension are significant parameters in the design of CMOS based IC design. Most analog circuit reduction in terms of size as parameter typically describes solitary or many objectives-controlled optimization issues. The eminent challenges with regards to size and power dissipation can be described as problems that are typically encountered under certain conditions. In this study, the design of a two-stage CMOS Differential Amplifier applying the nature-inspired Grey Wolf Algorithm for optimizing the area and power is utilized. To enhance the formulation terms concerning important considerations such as the amount incurred, strength, and functionality; a computerized formulation approach is used. This formulated design proposal will meet specifications such as positive and negative Slew Rate, Unity Gain Bandwidth and Phase Margin, etc. Chaos theory can be induced into the Grey Wolf Optimization Algorithm (CGWO) with the help of speeding global convergence metric i.e. Speed. The results obtained from CGWO are then analyzed with the functionality of other prevailing optimization techniques employed in the analog circuit sizing. Depending on the investigations, CGWO functions reduce the dimensions of the circuit and analyze the prevailing techniques by achieving a healthier rate of convergence and power dissipation with low value.**

Keywords—CMOS; CGWO; optimization technique; operational amplifier; aspect ratio; power dissipation

I. INTRODUCTION

The development of expertise, compact devices, and special equipment have brought a tremendous change and enhanced an individual's style of living. Apart from this the prospects in the added formulation, characterize greater throughput and lengthier duration of a battery lifetime. Inexpensive memory, enormous processing strength, and rapid linking of packs are due to the determination of the semiconductor industry that has been following Moore's Law

for more than a few decades. As the CMOS device becomes smaller, the design of a circuit increases in performance and dissipates low power [14]. IC's with 14nm fabrication techniques are used in the process of fabrication. IC Manufacturers are involved in researching the formulation of circuits in 7nm fabrication techniques. EDA based mechanisms support in identifying the best possible formulation techniques for reducing the power consumption adopting a strategy for reducing the dimension of gate sizing and choice of V_T. Engineers spend their considerable energy concentrating on the choice of software to formulate a devising strategy that satisfies formulation challenges. In addition to attaining the power objectives in the requirement, present electronic design software available in the market functions with a certain percentage of power reduction. It may not sufficiently explain the case where it originates in employing the strategy that satisfies the frequency needs utilizing reduced power in a global circumstance [13]. Mixed-Signal designs are growing rapidly in quantities such as a huge portion of fresh Integrated Circuits (IC's) that desire a need for connection to the outside world. With the incessant upsurge in the density and functionality of IC's, minimizing the dissipation of power has provoked a thoughtful challenge. A circuit engineer should be ready to face the challenge and be able to come up with the optimum design of the circuit. Simultaneously the inconsistent surge in various important technical characteristics might considerably upset the formulation and attainment of correct and least power consumed ICs in nanometer arrangement [11]. Gate Sizing Optimization is crucial to obtain timing closure and minimize the power dissipation of integrated circuits [12].

In the process of progressing towards technology, the chip manufacturing designers are subject to numerous technical obligations. Still, semiconductors consider power consumption and power dissipation as fundamental issues in the design of analog IC for the present scenario and may continue to do so for the future years. The latest problem that is being faced by the industry is dependability that comprises of production-connected disparities in addition to internal and external disturbances. The dissipation of power of a CMOS gate comprises two mechanisms i.e. stationary and active [16]. The stationary power dissipation is because of the movements of current in the supplies (VDD and GND) though devoid of switching process in the circuit. Because of a minor portion of

the current that leaks through the reverse-biased junctions of the transistors, static power dissipation's non-conform to a perfect zero. The charging and discharging of the capacitive load have resulted in the dynamic power dissipation. During the changeover from low to high, the pMOS transistor(s) scatter energy and while from high to low changeover, the nMOS transistor(s) scatter energy. Static Power can be explained with a changeover of the gate in between ON-state and OFF-state with a given frequency. Power-Delay-Product (PDP) is utilized in an explanation of the dissipation of power [15].

Comprehensive system-on-a-chip is developed by incorporating assorted analog and digital circuits with the help of experts that are advancing in the field of VLSI. In a complete circuit, though the analog fragment takes up only a small proportion it has a greater complexity in devising better circuits because of the toughness that requires comprehensive expertise in the behavior of circuits. Computerized utilization in the selection of dimension strategy gets affected because of lengthier duration and greater complexity of formulation. This arises due to incompetent expert practitioners. This results in attracting greater challenges in computerized synthesis strategies of circuits. The formulation of processes depends on the structure and its parameters. The present study focuses on the design of circuits using parameters concentrating on the choice of parameters and finding the best solutions with the help of optimization techniques to enhance the functionality of pre-designed circuit structure [18].

In the design of analog ICs, the most important motivations i.e. Size -based methodology is explained here as follows: The first and foremost one explains substitution of search of tiresome and unstructured labor-intensive compensation by the instinctive formulation of parameters. In the second method, it helps to determine solutions to problems that are complex to formulate by hand. Preciseness, simplicity, generalization, sturdiness, and satisfactory duration are the parameters to be assessed for execution to improve the synthesis of the circuit for achieving good standards for approval. Apart from the tough challenges that are faced by the engineers, satisfying the designer's necessities for extremely controlled challenges and the capacity to attain exceedingly augmented outcomes are important motivations for greater functionality in the proper selection of dimensions for the integrated circuits. Using various parameter-based formulation techniques, methodologies, and tools which are established in recent years, some of them have achieved good market status. Many Integrated Circuit dimensioning issues have articulated with the view of optimizing either the single or multi-objective-controlled constraint. This constraint explains the reason for the reduction of power consumption commonly focused on certain issues e.g. It was found that gain was larger with certain threshold values [17].

The reduction in the dimension of IC's is performed by adopting or following diverse strategies depending on the expertise of the designers and on many of the optimization techniques [19]. The fundamental concept of knowledge dependent design is intended towards devise formulation of expressions in a quantity that provides functionality features and formulation parameters that are easily evaluated. The

perception of an expertise-dependent selection of dimension methodology impacts the formulation expressions. Implementing tools for obtaining solutions concerning preciseness and sturdiness are often not satisfactory in tough circuits and contemporary techniques. This is due to the huge preliminary time needed to generate design tactics or expressions that could be a major disadvantage. Moreover, this complexity involves utilizing the energy in the selection of different techniques that are restricted towards a reduced group of circuit structures. By selecting the function optimizing techniques, the design strategy is modified to reduce the function and utilization of mathematical strategies to determine the best possible solutions. This type of technique is broadly recognized and accepted all over the world. Most prominently it is dependent on the definition of a functionality measurement within a repetitive optimization loop [20].

II. Literature Survey

Optimization of VLSI circuits needs evolutionary techniques because of the simplicity and ease of approach. In the paper proposed by Sarkar *et al*. (2018) [1], the aim of achieving this dimension is optimum and the purpose of obtaining reduced offset voltage in the formulation of two-step CMOS OP-amp is accomplished with the help of Whale Optimization Algorithm. The proposed design satisfying diverse formulation conditions like Slew Rate, Open Loop Gain, etc. will be considered as additional conditions in the design of the operational amplifier. To manage current disparity during the output stage of the Operational Amplifier, offset reduction is considered to be a significant need. Subsequently, by reformulating the Operational Amplifier in the usual CADENCE Virtuoso circuit simulator, technical outcomes of the process are confirmed. The results of simulated outcomes and the outcomes obtained through the Whale Optimization Technique are well identified. The outcomes derived through the proposed WOA are then analyzed with the functionality of some other techniques utilized in the previous research papers. It is observed that the WOA achieved better results for the circuit dimension with the lowest size in the design of CMOS Operational Amplifier for reduced offset as analyzed with other techniques. Based on the comparative analysis, it is found that WOA outclasses all the other techniques by achieving a faster convergence, least power dissipation and reduced offset.

For enhancing the cost-effectiveness in the formulation procedure of analog ICs, stability, and functionality, the computerized design procedures are employed. The occurrence of boundaries in the disturbance, the minimum strength of the signal at a circuit can be managed to a satisfactory level but it upsurges the difficulty of the circuit design. Optimization techniques consume a lot of time for finding the solutions and complex processes that encompass managing broader diversity of inconsistent limitations or design conditions and broader expanse of characteristics in the design process.

Work proposed by Singh *et al.,* (2018) [2] suggests overcoming the above-mentioned limitations by implementing Particle Swarm Optimization with an Aging Leader

(ALCPSO)-dependent formulation technique. Concurrent reduction of thermal noise and the dimension of the circuit was the prominent focus of the researchers in the proposed work. For achieving that, ALCPSO is utilized in exploring the solution inside the space that is provided for processing the conditions along with the characteristics that are useful in the formulation of the circuit. On the other hand, the established strategy for formulating the circuit includes reduction of distortion due to thermal effect as one of the prominent design conditions along with other conditions that are missing in the preceding computerized technique. The established technique aims at reducing the dimension such as length and breadth that consequently reduces the area of the circuit. The evaluation of the ALCPSO-design technique was carried out by utilizing MATLAB. To synthesize in the CADENCE tool with 0.18 μm parameters technique is used for examining the proposed technique by utilizing the ALCPSO method.

Most prevailing technologies utilized either Logical Effort (LE) strategy or individual optimization techniques for computerized selection of dimensions of the transistor for the CMOS logic circuits. A logic circuit is optimized only following the speed while it completely avoids power and dimension by the Logic Effort Strategy. A large amount of processing exertion is required while heuristic algorithms are utilized as the only individual technique for optimization purposes. Enforcing constraints on the dimensions of the transistors in such a way that it would help in reducing the strategical space satisfies the conditions of the destination.

In the paper proposed by Kunwar Singh *et al*., (2018) [3] the above challenges were overcome by employing latency factor of sensitivity depending on the theory of Logical effort methodology as devised by Alioto *et al*., to predict the maximum functioning speed of a logic circuit in addition to finding the maximum limit of the transistor's dimension. To confirm the efficiency of the recommended technique PVT investigation and Monte Carlo simulations were utilized.

For the formulation of optimal strategies for two of the normally utilized analog circuits, such as CMOS differential amplifier with current mirror load in CMOS, two-step Op-Amp, a hybrid population dependent meta-heuristic search technique called as Gravitational Search Algorithm (GSA) was incorporated along with Particle Swarm Optimization (PSO) (GSA–PSO) by Mallick *et al*., (2017) [4]. PSO and GSA belonged to the modest population dependent strong evolutionary technique, but on the other hand, they contain one of the issues i.e. sub-optimality. For the accomplishment of optimal strategies of two amplifier circuits, the formulated GSA–PSO dependent technique was utilized in overcoming this disadvantage confronted in PSO and the GSA techniques and was implemented by Mallick *et al*., in his research work. The dimensions of the transistors are optimized utilizing GSA–PSO in such a way that it reduces the dimensions engaged by circuits and enhances the design/functional characteristics in the circuits. For optimizing the dimensions of transistor sizes, several design constraints/functional characteristics are taken into consideration. To validate the dominance of GSA–PSO over the other optimization techniques by the speed of convergence, formulation constraints and functionality characteristics in the optimal

formulation of the analog CMOS amplifier circuits, the simulation was performed, and comparative investigations were done. Some more issues and problems confronted by the research carried out by Mallick *et al*. had an appropriate adjustment in regulating characteristics by the GSA-PSO technique. Certain contradictory formulation/functionality characteristics were moderately mitigated with the help of frequent physical adjustments. To overcome the above-mentioned complex issues, utilization of Multi-objective optimization is preferred as a replacement.

For the quick selection of optimum dimensions of CMOS Analog Circuits utilization of the substitution modeling strategies along with a grouping of meta-heuristics was projected in the research work carried out by Garbaya *et al*., (2018) [5]. Utilization of meta-modeling techniques within an optimization loop and demonstrating the benefits as their primary motivation. They had taken into consideration the design of two CMOS analog circuits in addition to demonstrating techniques that permit the accomplishment of the selection of optimal dimensions. The traditional in - loop optimization strategy achieved the mentioned functions with minimum processing duration. The achieved outcomes depicted that the RBF-PSO technique permits in achieving outcomes as precise as the ones achieved by utilizing the traditional in-loop optimization strategy, but with a substantially minimized duration for the execution of the proposed technique.

The prominent reason for power dissipation is due to the power leakage in the circuit that is designed with the nanometer technique. The most utilized renowned technique in the minimization of Power leakage is the Input Vector Control (IVC). Because of the impact of stacking strategy that is utilized in IVC, this technique provides Leakage Power that will be minimum for the Minimum Leakage Vector (MLV) enforced as sources of the circuit under inspection.

To determine the leakage vector with a minimum value, Particle Swarm Optimization (PSO) technique was utilized in research work performed by Rani, and Latha (2016) [6]. The genetic Algorithm was also utilized to explore the Leakage Vector with the Minimum objective and analyzed with PSO concerning the number of steps utilized in the optimization. Simulation outcomes were observed and it demonstrated that PSO reliant technique performed superiorly in the determination of Leakage Vector using minimum value when compared with the GA method because PSO procedure utilizes the least quantity of duration of execution related to GA. PSO based Optimization technique in determining the leakage vector with minimum value and in the optimization of power leakage was proposed and utilized for the first time.

In the paper proposed by Azam *et al.,* (2016) [7], a methodology for simultaneous optimization was formulated for CMOS logic gates for power-and-noise margin and energy-and-noise-margin. The sizing parameter for functionality improvement of various gates had been extended to satisfy other figures of merit, such as dependability, power, and energy. By utilizing the examples of three and four input logic gates, they have explained how multiple yet contradictory formulation objectives can be obtained. For

example, one of their high functionality gates showed power savings of more than 30% while minimizing the gate area by 39%. A significant stage of compromising the rise and fall times of outcome was also utilized in the optimization framework. Their formulated technique was expandable, and it could be utilized for optimizing greater logic blocks. Even though developing gate sizing methodology was motivated to enhance functionality, the present research discloses many other benefits of the methodology. The expandability of their methodology and the inspiring outcomes had made them examine complex and bigger CMOS circuits.

Opposition Dependent Harmony Search technique (OHS) was utilized in the research by Maji *et al.*, (2015) [7] for the formulation of Differential Amplifier with CMOS Transistor in an optimum manner. With the help of rules such as memory rule, a pitch fine-tuning rule, and an initialization procedure, every answer in Harmony Memory (HM) produced provides the best outcome with the smallest possible error fitness in n-dimensional exploration spaces. Compromise in the investigation and taking advantage of the utilization of exploration space resulted in the Integration of various regulating characteristics using fundamental HS technique. The disadvantages of early convergence and sluggishness are reduced by utilizing the OHS technique in the formulation of CMOS Differential amplifier. SPICE simulation is implemented on optimized characteristics for assuring the dominance of OHS based strategy outcomes to the rate of convergence formulation criteria and motivations observed assure the dominance of the formulated OHS based technique over other optimization techniques in the formulation of designed amplifier in an optimal manner. Apart from showing dominance for the various parameters, the suggested technique delivers a reduction in dimension of the transistor along with enhanced gain and scatters power reduced in comparison with the observed existing researches.

For any circuit application, while manufacturing chip minimization area forms the fundamental objective in any circuit design procedure; the formulation phases encompass a simulated process for recognition that is performed repetitively for their effectiveness. For this motivation, the CAD algorithms provide a diverse solution based on the requirements and constraints formulated by the engineer. EDA tools help in the conception of impacts created by proposed algorithms over the functionality of circuit functionality in addition to the measurement of floor dimension engaged while designing the circuit.

The research work proposed by Swetha *et al.*, (2015) [8] explains the impact of hybrid strategy for formulating the proposed circuit. The proposed work explains the impact of enforcing the navigation reliant aggregating techniques KL, FM for the circuits thus optimizing cells utilized by the Hybrid Genetic Algorithm (HGA).

For optimizing the analog IC, a constrained sparse modeling technique was implemented in the paper proposed by Tao *et al.*, (2018) [9]. This paper described the collective benchmark circuit employments at gate level optimizing the dimensions of transistors utilizing evolution dependent GA technique. A segregation and deployment node in proper position and uniting the formulation phases of floor planning and segregation of nodes is performed by the proposed hybrid Genetic Algorithm. The outcomes recommend such a technique, on the formulation of circuits that offer possibilities of integrating the phases of physical design stages of partitioning with the deployment of nodes in addition to optimizing the dimension of the transistor in the formulation procedure.

For optimizing the analog circuits within the local formulation space, by efficiently employing convex semidefinite programming relaxation the above-mentioned prototypes are utilized. Formulated Prototype and optimizing strategy might rapidly converge towards an accurate solution for the design of analog IC's by utilizing mathematical samples as compared to the traditional techniques that fail in the proper functioning of the circuit. A limitation of an acyclic graph can be fulfilled by taking into consideration the GC-SPM. They were able to demonstrate it with the help of a group of scarce functionality representation. To achieve global optimum with least processing expenditure and memory utilization, optimization technique might complement with convex SDP relaxation technique. Their mathematical analysis established the effectiveness of the formulated strategy on performing comparative analysis with a traditional sparse POP strategy. With the help of transistor-level simulations, the toughness of the formulated optimization technique depending on GC-SPM was simulated. Effective strategies for minimizing the number of simulations needed to model the precise functionality or execution of every simulation with pronounced significance might analyze their upcoming investigation. Moreover, to optimize the enormous framework, they might prolong the formulated strategy in determining solutions for optimizing the issues of multi-objective nature and obtain Pareto Optimal fronts to separate the analog blocks.

Depending on the physical characteristics based on g_m / I_D as a guide for the optimization strategy of the power dissipated, the least value for the analog CMOS ICs is proposed by Girardi and Bampi (2006) [10]. ACM MOS bunched and solid model in the optimization loop is implemented with the help of the conventional layout tool LIT implements. To achieve the answers nearer to an optimum solution with solitary technique reliant on a curve and precise equations for the parameters such as transconductance and effective current within the complete functional areas is carried out with the help of the strategy utilized for computerized design within LIT and takes advantage of entire formulation space by using the simulated annealing optimizing procedure. This procedure contains an investigative equation that is incessant in the present conditions, comprising feeble and modest inversion utilized by the strong and bunched prototype that supports the best solutions and employment in an optimized manner. Benefits in limiting optimization strategy inside the power budget take pronounced significance for the transistor to have the least power consumption. Samples that depicted the optimization outcomes are achieved with LIT, leading to considerable power savings. The formulation of a folded cascade and a two-stage Miller Operational Amplifier was possible.

III. PROBLEM FORMULATION

An optimization problem with constraints takes the subsequent arrangement:

$min_x f(x)$

Subjected to

$g(x) \geq 0$

$h(x) = 0$

$X_L \leq x \leq X_U$

The value of a function is optimized to be the objective function f(x). Here, g(x) and h(x) are the in-equivalence values with equivalence constraints. X_L and X_U are the limits of variables. While achieving the solution, certain conditions might fulfill the equivalence conditions. These constraints are known to be active constraints while others are known to be inactive constraints. The active constraints compose the active set.

Formulation of a circuit takes the following formats so that an op-amp could be devised as an optimization problem with constraints like subsequent statements.

$Min_x Area(x)$

Subject to

$Gain(x) \geq GAIN$

$Slew\ Rate > SLEW\ RATE$

$Unity\ Gain\ Bandwidth \geq UGB$

$Phase\ Margin \geq PHASE\ MARGIN$

$X_L \leq x \leq X_U$

The design variables x are the bias voltages and represent currents and dimensions of the device. The functions Gain, Slew Rate, etc. are considered as nonlinear functions in a certain or complete set of variables. Formulation conditions are marked in capital letters on the right-hand side of the conditions in equations [27].

Answers for certain problems in optimization are not well defined [21]. Equivalence conditions and in-equivalence conditions are characterized usually as numerical equivalence and in-equivalence expressions correspondingly for the problem of optimization. Parameter variations are to be satisfied in both classes of conditions. Deterministic techniques such as viable route strategy in addition to comprehensive gradient descent techniques are generated to determine solutions to limitation issues [22]. These techniques are not effective while considering real-time applications that comprise of structural optimization problems. To handle these complex conditional issues several metaheuristic algorithms are devised. These techniques intended towards the bearable velocity of convergence, improved accuracy, robustness and enhancement of functionality

IV. PROPOSED METHODOLOGY

The operational amplifier is an outstanding device out of the available electronic hardware. Operational amplifiers operate at several stages of multifaceted excellence that needs to be utilized in the process of recognizing capabilities ranging from a forthright DC inclination generation to swift improvements or isolation. Operation amps are the most widely employed construction hampers in Analog and Digital Electronic Circuits that are most normally employed as a portion of used electrical and logical devices [30].

In the formulation of a two-stage operational amplifier (op-amp), folded cascade Operational Trans-Conductance Amplifier (OTA), etc. the differential amplifier features a regular analog portion and takes the most prominent stage. Analog IC manufacturing technique is fundamentally decomposed into three important stages:

- Adoption of Proper circuit topology

- Optimized Sizing for the Device

- Extraction of proper Layout

The formulation procedure encompasses two prominent steps: conception of formulating technique and optimization of selected techniques. The visualization of the design is carried out with the help of recommending architecture to satisfy the provided conditions. The visualization step is usually carried out with the help of manual calculations to handle the spontaneous viewpoint required to satisfy the selections that must be followed. Considering the "First Cut" design; examining it and the optimization of the design technique is the subsequent step. The second step is usually performed with the help of computer simulation and can comprise of stimulus from conditional or procedural fluctuations.

The generation of proper physical formulation and the development of Low power Op-amp is our key focus. The characteristics of an ideal op-amp containing a single-ended output are listed as the ideal op-amp. It should have differential input, infinite voltage gain, infinite input resistance, zero output resistance. But in real circumstances, the above-mentioned parameters might not get satisfied. On the other hand, the functionality of the op-amp should be adequate for the good performance of the circuit and nearly achieve the parameters prescribed for ideal conditions when being applied to many applications. Every fresh evolution of the CMOS process establishes the formulation of op-amps that endures in bearing the additional conditions in such a way that the supply voltages and the channel length of the transistor are reduced [29].

It is possible to carry out the devising strategy of analog IC and the selection of proper dimensions with the help of skillful engineers and utilizing insight and knowledge. The exploration space intensifies, when the circuit complicatedness grows, and it is much complex to formulate analog ICs. Therefore, the formulation procedure takes a long time for engineers to achieve closer ideal parameters. So, engineers rely more on optimizing techniques. In the procedure of formulation, the optimal formulation of analog

components is a serious challenge. Appropriate selection of device dimension is very significant for dependable, effective and accurate CMOS Analog ICs formulation. Device dimensions and the inter-association between the Aspect Ratios of MOS transistors provide the assurance of the exploration space in the devising strategy of CMOS Analog IC. Analog IC devising strategy and proper selection of circuit dimensions and selection of efficient optimization strategies is an important prerequisite.

In 2014, Mirjalili *et al*. introduced an influential and powerful meta-heuristic nature-inspired optimization technique, known as Grey Wolf Optimization (GWO) [23] that relies upon grading in the community, leadership profile in addition to natural hunting performance of the mentioned animal community. The Grey Wolf Optimization meta-heuristic techniques contain the capability of circumventing local optima stagnation to a certain amount [27] and reliant on the generation of the population. Along with the above-mentioned advantage, it has a superior convergence rate in the achievement of the optimal solution that navigates automatically towards the optimal solution by powerfully exploiting the search space. Nevertheless, the utilization of a global search technique was not exploited comprehensively. Thus, in some cases, GWO flops in the identification of globally best solution in certain circumstances. Because of the above-mentioned fact, some of the issues cannot be managed by GWO in a competent manner [28].

Chaos theory was enforced in various applications by the progression of non-linear dynamics [24]. It also efficiently combines with the optimization strategies [25]. Various Meta-heuristic Optimization techniques along with the effective combination of Chaos theory were being utilized which improve the performance to a greater extent [26].

A. Design Specification and Design Steps

Formulation conditions take the maximum share of significance in formulating any analog ICs. The pictorial representation of a two-stage Operational Amplifier is presented in Fig. 1. The conditions provided in the design of a differential amplifier are as follows:

1) Slew Rate (SR) in V/μs,
2) Small-signal DC voltage gain (Av) in dB,
3) Cut-off frequency (f-3dB) in kHz,
4) Maximum Input Common-Mode Range (ICMR) (VICMR (max)),
5) Minimum ICMR (VICMR (min)) in V,
6) Power dissipation (Pdiss) in mw
7) Phase Margin in dB

Channel Width and Channel Length of MOS which determines the aspect ratios(S) of MOS transistors, Load Capacitance (CL) in pF and Compensation Capacitance (CC) in pF are measured to be formulation variables of the differential amplifier. Various Phases of Formulation are employed by utilizing a connection following the conditions provided for the design. For achieving the appropriate channel width and Channel Length which helps in the selection of aspect ratios of entire MOS transistors is focused at reducing the area engaged by all the MOS transistors in addition to the

reduction of total power dissipation, it is implied that framing of Objective Function or Cost function will be most compulsory one.

8) Design Strategies adopted in the formulation of proposed Amplifier Circuit

Steps utilized in the design of the proposed circuit that is differential amplifier utilized in the Operational amplifier circuit will be provided by calculating according to (1).

$$\text{Let } L_1 = L_2, L_3 = L_4, L_5 = L_6 \tag{1}$$

Based on the anticipated phase margin, picked up least possible values for *Cc*, i.e. for a 60° phase margin, it is assumed that Right Half Plane (RHP) zero (z) is more than ten times to unity gain bandwidth (UGB).

$$z \geq 10\text{UGB} \quad \text{and hence assume that } C_c \geq 0.22 C_L \tag{2}$$

The value of I_{D5} is found out to meet the Slew Rate as shown in (3).

$$Slew\ Rate = \frac{I_{D5}}{C_L} \tag{3}$$

The minimum value of the tail current (I_5) is calculated as shown in (4).

$$I_5 = \text{Slew Rate} * C_c \tag{4}$$

Tail current (I_{SS}/I_5) can be calculated as in (5).

$$2 * \pi * f_T = \frac{2 * I_{SS}}{(V_{GS} - V_{TH})^{\frac{1}{C_L}}} \tag{5}$$

Where I_{ss} is the tail current. The value of the Aspect ratio for fifth transistor S_5 is computed from the least input voltage. The value of V_{DS5} (sat) and S_5 is calculated subsequently as shown in (6) and (7).

$$V_{DS5}(\text{sat}) = V_{IN}\ (\text{min}) - V_{ss} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max})100\ \text{mv} \tag{6}$$

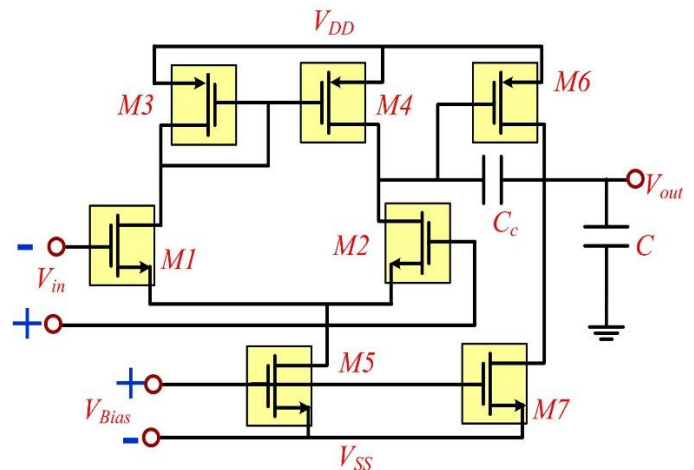$$S_5 = \frac{2 * I_5}{K'_5 [V_{DS5}\ (sat)^2]} \tag{7}$$

Fig 1. Schematic of Proposed Amplifier.

The value of S_6 is calculated by making the second pole (p2) equivalent to the product of 2.2 * Gain Bandwidth Product and making an assumption by which $V_{SG4} = V_{SG6}$ as shown in (8) and (9).

$$I_6 = (S_6 | S_4)I_4 \tag{8}$$

For balancing, I_6 must equal $I_7 = \frac{S_6}{S_7} = \frac{2*S_7}{S_4}$ $\qquad$ (9)

Calculating the aspect ratio of the first transistor that is equal to the second transistor to meet the voltage gain $\frac{W_1}{L_1} = \frac{W_2}{L_2}$

where first stage gain is given as in (10).

$$A_{V1} = g_{m1} * R_{OUT} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2}{\lambda_n + \lambda_p} \left(\sqrt{\frac{K_n'*W_1}{I_{D5}*L_1}} \right) \tag{10}$$

The second Stage gain is obtained as in (11), (12), (13) & (14).

$$A_{V2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6 (\lambda_6 + \lambda_7)} \tag{11}$$

$$g_{m6} = 2.2 * g_{m2} \left(\frac{C_L}{C_c} \right) \text{ and } S_6 = S_4 * \left(\frac{g_{m6}}{g_{m4}} \right) \tag{12}$$

$$I_6 = \frac{g_{m6}^2}{2*K_6'*S_6} \tag{13}$$

$$f_{-3dB} = \frac{1}{R_{OUT} * C_L} \tag{14}$$

Aspect Ratio of the third Transistor is calculated that is equal to the fourth transistor $\frac{W_3}{L_3} = \frac{W_4}{L_4}$ to determine and meet the upper Limit of ICMR as shown in (15) and (16).

$$V_{lc} (\text{max}) = V_{DD} - V_{SG3} + V_{in1} \tag{15}$$

$$\frac{W_3}{L_3} = \frac{2*I_{D5}}{K_p' (V_{GS3} + V_{tp})^2} = \frac{W_4}{L_4} \tag{16}$$

Aspect Ratio of Fifth Transistor is estimated $\frac{W_5}{L_5} = \frac{W_6}{L_6}$ that is equal to the sixth transistor to find and meet the lower limit of ICMR as given in (17) and (18).

$$V_{lc} (min) = V_{ss} + V_{Ds5}(sat) + V_{Gs1} = V_{ss} + V_{Ds5}(sat) + V_{Gs2} \tag{17}$$

$$\frac{W_5}{L_5} = \frac{2*I_{D5}}{K'_n [V_{DS5} (sat)^2]} = \frac{W_6}{L_6} \tag{18}$$

I_{D5} is measured to meet the power dissipation P_{diss} where

$$P_{diss} = I_{D5} (V_{DD} + |V_{SS}|) \tag{19}$$

$$P_{diss} = (I_5 + I_6) (V_{DD} + |V_{SS}|) \tag{20}$$

Right Half Plane Zero (RHP zero)

$$z_1 = \frac{g_{m6}}{C_c} \tag{21}$$

The calculated root is very unwanted as this one increases the amplitude while declining the phase leading left-half plane pole as in (22).

$$p_1 = - \frac{(g_{ds2} + g_{ds4})*(g_{ds6} + g_{ds7})}{g_{m6}*C_c} \tag{22}$$

This root completes the anticipated compensation Left half-plane output pole $p_2 = - \frac{g_{m6}}{C_L}$ $\qquad$ (23)

To fulfill the phase margin, the calculated pole must be greater than the unity-gain bandwidth 60 Degree phase Margin as given in (24).

$$g_{m6} = 2.2 * g_{m2} \left(\frac{C_L}{C_O} \right) \tag{24}$$

For Optimization, the design of Objective Function is the most crucial stage and optimization algorithm will maximize or minimize the objective function called Cost Function depending on the constraints and the focus primarily is on determining the best feasible solution by satisfying all the provided conditions. Objective Function may be single or multi-objective [31].

In equation (25), Objective function or Cost Function can be calculated as:

$$OF \text{ (or) } CF = \sum_{i=1}^{n} (W_i * L_i) \tag{25}$$

Where *n* represents the number of transistors utilized in the formulation of the total circuit, 'W' represents the width of the MOS transistor and L represents the length of the MOS transistor. The primary motivation lies in optimizing the value of *Objective Function* which has to be smaller than 180 μm² for the provided circuit configuration.

B. Grey Wolf Optimization

Mirjalili *et al*. [23] introduced and established The Grey Wolf Optimization (GWO) technique that exploits the behavior of headship grading and chasing and attacking strategy of the prey by grey wolves in wildlife. These animals have their place to the Canidae family that are taken into consideration and takes its position as prowler in the highest point of the food cycle. Their social leadership grading is divided into alpha (α), beta (β), delta (Δ) and omega wolves (Ω).

The grey wolves contain various types of clusters intended towards diverse activities like framing a cluster to accommodate and pursue the target. Grey wolves that take the position as uppermost status in the arrangement are known to be alpha category wolves and these will be measured as the front runner in the bunch. These categories of wolves are involved in policymaking, power attacking, chasing, napping and period to awaken, etc.

Category of the above-mentioned animals that take a position as the second level in the ranking order is known to be beta category and are second only to the alpha category. Beta Category supports the alpha category in the policy composting process. In circumstances where alpha category wolves are becoming aged and unfit to lead the group or expire suddenly, then beta wolves take up the position as leading the group in the place of alpha wolves.

The wolves that take the position as third in the order of the hierarchy are supposed to be called as the omega kind of wolves. They continuously track the commands provided by the dominant category of wolves, alpha and beta wolves in the ranking. Thus, Omega sort of wolves is compulsorily required

in maintaining the superiority assembly in the order [32] and maintain discipline among the group.

The category of wolves that is not fitting itself in the alpha, beta and omega class of the mentioned animals will be determined as delta class of wolves. Delta categories incessantly obey the alpha and beta categories of wolves, on the other hand, try to dominate the omega category of wolves.

All categories of wolves are divided into five fundamental kinds of wolves based on their operation and functionality. They are listed as following (i) Scouts, (ii) Sentinels, (iii) Elders, (iv) Hunters and (v) Caretakers.

Scouts are accountable intended towards the inspection of the borders in addition to conveying the cluster about the threat. Sentinels are intended towards assuring the security of the cluster. The elder category of wolves takes up the position as knowledgeable wolves and the knowledge provided by them is utilized for ambushing the target or identifying the elements. Functions such as Hunting the target and offering the food for the cluster are taken up by the Hunters. Lastly, Caretakers are accountable for taking care of the fragile, hailing and wounded animals. To explain the hunting strategy of the mentioned animals four diverse phases are utilized.

1) Searching for prey: Exploration procedure started with any arbitrary way of beginning of candidate solutions from the examination space. They deviate from one another to probe the target and congregate after they identify it.

2) Encircling prey: After identification of the target, grey wolves enclose the target. Encircling conduct might be signified as specified below in (26) and (27).

$$\vec{E} = |\vec{O}.\overrightarrow{Xp}(i) - \vec{X}(i)| \tag{26}$$

$$\vec{X}(i+1) = \vec{X}_p(i) - \vec{B}.\vec{E} \tag{27}$$

Here recent iteration is characterized by $\vec{B}$ and $\vec{O}$. These are the coefficient vectors. $\vec{B}$ is utilized in upholding the distance from search agents to the target. $\vec{O}$ signifies hindrances in the attacking route undertaken by animals whereas tactics in reaching the target. $\vec{X}$ signifies the position vector of the grey wolf besides $\vec{X}_p$ designates the position vector of the target.

The coefficient vectors $\vec{B}$ and $\vec{O}$ expressed as given in the equations respectively in (28) and (29):

$$\vec{B} = 2*\vec{l}*\vec{r}_1 - \vec{l} \tag{28}$$

$$\vec{O} = 2*\vec{r}_2 \tag{29}$$

While $\vec{l}$ shrinks proportionally from 2 to 0 at the time of iterations $\vec{r}$ and 1 and 2 will be arbitrary vectors within the range [0, 1].

3) Hunting: Subsequently, with the surrounding of the target, they are focused on hunting the target. The process of hunting normally is directed with the help of α, β & ϒ categories wolves. Out of these, 'a' delivers the finest candidate answer. Mathematically, the hunting performance of

the mentioned animals will be expressed as given from (30) to (36).

$$\vec{E}_\alpha = [\vec{O}_1 \vec{X}_\alpha - \vec{X}_i] \tag{30}$$

$$\vec{E}_\beta = [\vec{O}_2 \vec{X}_\beta - \vec{X}_i] \tag{31}$$

$$\vec{E}_\Upsilon = [\vec{O}_3 \vec{X}_\Upsilon - \vec{X}_i] \tag{32}$$

$$\vec{X}_1 = \vec{X}_\alpha(i) - \vec{B}_1.\vec{E}_\alpha \tag{33}$$

$$\vec{X}_2 = \vec{X}_\beta(i) - \vec{B}_2.\vec{E}_\beta \tag{34}$$

$$\vec{X}_3 = \vec{X}_\Upsilon(i) - \vec{B}_3.\vec{E}_\Upsilon \tag{35}$$

$$\vec{X}(i+1) = \frac{(X_1 + X_2 + X_3)}{3} \tag{36}$$

4) Attacking prey: After the accomplishment of hunting, they try to ambush the target. Permission of the search agents by the GWO techniques i.e., wolves try to update their locations for attacking the prey and are provided as per the position of α, β and γ class of wolves. It supports generating a dependable solution. For explaining the model for reaching the target, two vectors $\vec{a}$ and $\vec{A}$ are taken into consideration. Therefore, $\vec{a}$ proportional shrinkages from 2 to 0 while the iteration upsurges in addition to the oscillations of $\vec{A}$ and also diminished by the $\vec{a}$. But $\vec{A}$ is an arbitrary value between [-a, a]. While $\vec{A}$ takes any arbitrary value within the range [-1, 1], the subsequent location of animal might indicate from its present location to the target location.

A. Chaotic Grey Wolf Optimization Algorithm

Even though GWO has a decent proportion of convergence mechanisms, it is not able to accomplish the global optimization which impacts the convergence mechanism under all circumstances. CGWO Algorithm is designed by efficiently combining the non-linear chaos theorem in the GWO technique to diminish the convergence impact and enhance the effectiveness. Chaos is defined as a deterministic and arbitrary technique established in a non-linear, dynamic framework that is periodic, non-converging and constrained. Regularly, numerous combinatorial optimization problems are encountered, nevertheless, one should be ready to determine the solution for the related issue. This can include proper allocation of resources including time, strategizing the product delivery, devising the proper circuit, and computer wiring. The significant challenge in technology and engineering is the formulation of competent techniques for designing the solutions to these combinatorial problems.

Chaos is explained as the arbitrariness of an active framework and a chaotic system may be measured as the foundation for arbitrariness. Repeated chaotic neural networks are efficient for determining combinatorial optimization problems. Nevertheless, the technique cannot be enforced to very huge circumstances because it requires a large quantity of memory to build the design of the neural network. Because of the firing pattern of Chaotic Neural Network encoding of the solution, it is so much complicated to achieve the possible solutions. When the firing pattern of the neural network pleases the conditions then the solution is produced in that

circumstance. For determining solutions to the mentioned critical restrictions. Chaotic Neurons inspire heuristic algorithms [33].

Chaotic Dynamics is meticulously utilized in the employment of local exploration techniques. The fundamental component of the chaotic neuron is projected by Kitajima *et al*. [34]. Implementation of the local exploration algorithm is encoded by the firing of the chaotic neuron. If the chaotic neuron fires, the respective local search algorithm is implemented. Once the neuron starts firing, then the subsequent firing of the neuron will occur only after a finite duration. The firing process will be inhibited for a certain duration with the help of the assertiveness of chaotic neurons. It can be thus inferred that the recurrent firing of the neuron and regular accomplishment of the local search algorithm is circumscribed. Hence, chaotic exploration might efficiently avoid local minima. At that point, it stresses the fact by which impetuousness employed with chaotic neuron model results in similar or sometimes bigger resolving capacity than tabu search that contains a similar approach of exploring solutions as the chaotic exploration. Utilizing the aforementioned concept, chaotic search approaches are projected to determine the solution closer to optimality or estimated solutions for combinatorial optimization problems. Several chaotic maps containing diverse numerical expressions are utilized to combine the theory of chaos in optimization techniques.

Chaotic maps were extensively utilized along with the optimization area for the preceding ten years because of its dynamic nature that aid the optimization techniques in investigating the exploration space more vigorously and globally. A broader variety of Chaotic maps were formulated by engineers, investigators and specialists in the field of statistics in agreement with several human protectorates presently obtainable in the area of optimization [35]. Out of the accessible chaotic maps, a major portion was frequently enforced in optimization techniques to utilize in real-time circumstances. Ten appropriate single-dimensional chaotic maps utilized in this research work as gathered and analyzed from the available literature to confront CGWO is listed in Table II [36].

Any arbitrary number within the specified range of [0,1] might be selected as a starting value in those chaotic maps. However, it must be compulsorily observed that the starting value is creating pronounced effects over the oscillation pattern of certain maps. A diverse group of chaotic maps with the starting value as 0.7 is picked for utilization for all parameters [37]. The convergence mechanism of the GWO technique is getting affected by utilizing Chaotic maps completely along with the optimization as the maps influence the possible area of the GWO technique using Chaos non-linearity. Initially, the maps are anticipated to perform on the GWO only for a brief duration, but the effect prevailed stochastic for a longer duration. A brief algorithm explaining the projected CGWO algorithm for determining the solutions of optimization problems is established in Fig. 3.

For adjustment of key parameter 'a' which is critical in determining the convergence speed and improving the Location of Grey Wolves, the functionality of ten diverse chaotic maps was utilized and examined. Two-stage OP-AMP is formulated for 180nm technology as provided in Table I as per the subsequent requirements.

TABLE I.   DESIGN SPECIFICATIONS

Parameters	Values	Parameters	Values
Open Loop Gain	≥ 100V/V (40 dB)	Trans-conductance of PMOS K'$_P$	$(\frac{\mu_p C_{ox}}{2}) = 35.6$ µA /V^2
Slew Rate	≥ 10 V / µs	Threshold Voltage of NMOS V$_{tn}$	0.35 V
f$_{-3dB}$	≥ 5MHZ	Threshold Voltage of PMOS V$_{tp}$	-0.39 V
Load Capacitance	≥ 10 pf	Phase Margin	≥ 60 Degree
Positive Supply Voltage V$_{DD}$	2.5 V	CMRR	≥ 60 dB
Negative Supply Voltage V$_{SS}$	-2.5 V	PSRR	≥ 60 dB
Power Dissipation	≤ 2000 µ watt	Channel length modulation parameter for NMOS λn	0.09 / V
Common mode Input range	-1.5 V$\leq$ ICMR ≤ 2V	Channel length modulation parameter for PMOS λn	0.1 / V
Aspect Ratio	$2 \leq \frac{W_i}{L_i} \leq 100$	Trans-conductance of NMOS K'$_{N'}$	$(\frac{\mu_n C_{ox}}{2}) = 177.2$ µA /V^2

The Optimization Technique with Projected CGWO Strategy is provided in Fig. 2. Stochastic initialization of the population of grey wolves is carried out in this initial phase. In addition to the beginning of the process and selection, its initial chaotic number and a variable chaotic function that is required to be mapped with the GWO technique is also picked [35]. Consecutively, the parameters of the CGWO algorithm consisted of performing the exploration, – exploitation techniques, namely, a, A and C that will be like comparison with GWO. Within the exploration space, the fitness of all grey wolves is estimated utilizing several typical yardstick functions and are addressed by their fitness. After arrangement and organizing the first wolf is presumed as α wolf and consequently, second and third wolves are presumed to be β and γ wolf correspondingly. As a result, the fittest wolf shall be preserved by improving its location using Equation (36) and might obtain the location of α wolf as the best solution. As the progression of iterations using Equations (28) and Equation (29), the characteristic values get improved. Fitness of the Wolf is taken into consideration as the healthier solution determined by the CGWO technique after reaching the final iteration.

B. CGWO for Constrained Benchmark Functions

Two functions that are listed as Motivation Function and non-conformity of Constrains functions are utilized in the explanation of all the optimization problems with the set of conditions [39]. Objective function will be explained as the function that is having the foremost intention for determining the optimal solution say `x' in the particular exploration space. It is expressed in (37).

$$\text{Minimize } f(x), x = (x_1, x_2, x_3, \ldots x_n) \, \varepsilon \, R^n \tag{37}$$

where n is the number of dimensions that a solution is comprised of. $X \, \varepsilon F \varepsilon$ S in which F is the practicable region in exploration space S that explains an n-dimensional rectangle R [38]. The mentioned rectangle R has domain size within the range of lower limit (ll) and upper bound (ul) as signified in (38).

$$ll(i) \leq x(i) \leq ul(i), 1 \leq i \leq n \tag{38}$$

and the number of conditions to be satisfied are said m (m> 0) will be explained in the F space in Equation. (39).

$$g_j(x) \leq 0 \text{ for } j= 1,2,3\ldots q$$

$$h_j(x) = 0 \text{ for } j= q+1, \ldots\ldots m \tag{39}$$

Here $g_j(x)$ and $h_j(x)$ are termed as in-equivalence and equivalence conditions. If any solution says `x' pleases the condition g_k or h_k in F space, then g_k is measured to be a dynamic condition at x.

V. EXPERIMENTAL RESULTS

A. CGWO based Circuit Design

To achieve the best circuit sizing for two-phase CMOS Operational Amplifiers CGWO technique is applied. The optimal sizes of the MOS transistors along with Load Capacitance and Compensation Capacitance by minimizing the primary objectives that are power dissipation and area is performed by the proposed CGWO technique. Along with the operation proposed algorithm so that it satisfies specified formulation characteristics and conditions for the design. By manually identifying the power supply values and the characteristic values for the selected technology must be performed during the optimization procedure. The parameter values for the selected technology, values for the power supply and the boundaries of design parameters and specifications are provided as inputs for the Optimization Algorithm. Optimally Corrected solution for design parameters $((Wi/Li)$, C_C, P_{diss} in addition to the specifications for formulation (SR, A_V, $f\text{-}3_{db}$, V_{IC} (max), V_{IC} (min), C_L $OFFSET$), where $i = 1, 2, \ldots, 8$ is provided by the projected technique for two-step Op-Amp circuit using CMOS transistor chosen in the proposed papers. Schematic of two stage OP-AMP is shown in Fig. 4 and simulated using Mentor graphic technology and this technique is utilized invalidating the answers provided by the recommended technique.

Parameter values specified for the design proposal and the selected technology (180 nm) are presented in Table III. Simulations are carried out using the system with CPU Intel core i7 that contains 4 GB RAM and MATLAB. For the proposed CGWO algorithm, the total quantity of search agents selected is 50 and the dimension chosen is 10 i.e. the design variables picked for the proposed circuits are 7. The highest number of iterations selected for the recommended technique is 100. Schematic and Gain of the proposed two stage operational amplifier versus frequency is shown in Fig. 4 and Fig. 5. Also, Power dissipation versus time also shown in Fig. 6. Table II contains various chaotic maps and their corresponding expressions which are used in CGWO.

TABLE II.   LIST OF CHAOTIC MAPS AND THEIR EXPRESSIONS UTILIZED IN CGWO

| S.No	Name of the Maps	The expression for the map
1	Bernoulli map	$x_{k+1} = \dfrac{x_k}{1-a} \quad 0 \le x_k \le a$ $= \dfrac{x_k-(1-a)}{a} \quad 1-a \le x_k \le 1$
2	Logistic map	$x_{k+1} = a. x_k (1- x_k)$
3	Chebyshev map	$x_{k+1} = \cos(a \cos^{-1} x_k)$
4	Circle map	$x_{k+1} = x_k + b - \dfrac{a}{2\pi} \sin(2\pi x_k) \bmod (1)$
5	Cubic map	$x_{k+1} = p(1 - x_k^2) \quad x_k \, \varepsilon \, (0,1)$
6	Iterative chaotic map with infinite collapses (ICMIC) map	$x_{k+1} = \mathrm{abs}\left(\sin\left(\dfrac{a}{x_k}\right)\right) \quad a \, \varepsilon \, (0,1)$
7	Piecewise map	$x_{k+1} = \dfrac{x_k}{a} \quad 0 \le x_k \le a$ $= \dfrac{x_k-a}{0.5-a} \quad a \le x_k \le 0.5$ $= \dfrac{1-a-x_k}{0.5-a} \quad 0.5 \le x_k \le 1-a$ $= \dfrac{1-x_k}{a} \quad 1-a \le x_k \le 1$
8	Singer map	$x_{k+1} = a(7.86x_k - 23.31x_k^2 + 28.75 x_k^3 - 13.302875 x_k^4)$
9	Sinusoidal map	$x_{k+1} = a x_k^2 \sin(\pi x_k)$
10	Tent map	$x_{k+1} = \dfrac{x_k}{0.7} \quad x_k < 0.7$ $= \dfrac{10}{3}(1-x_k) \quad x_k \ge 0.7$
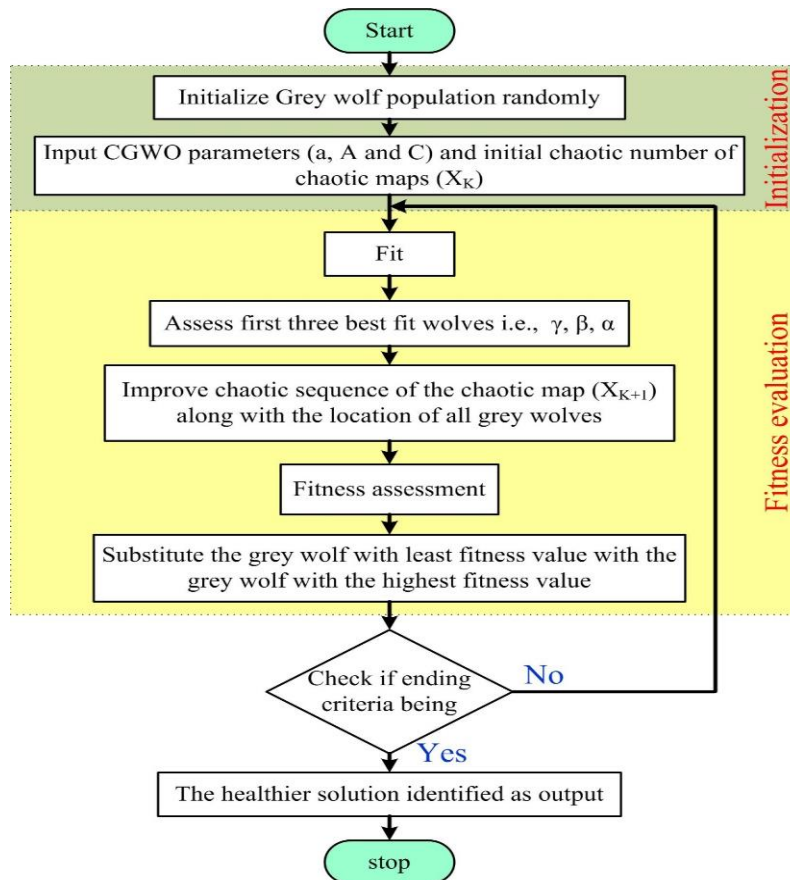
Fig 2.   Flow Chart of Optimization Using CGWO.

Initialize the generation counter t and arbitrarily start the population X_i of grey wolves X_i were (i =1, 2…. n)

Initialize the value of the Chaotic map x_o arbitrarily

Initialize parameters a, A and C

Determine the fitness of every wolf

X_α =The the best wolf

X_β =The second-best wolf

X_δ =The third-best wolf

While (t < Max_ iterations)

Organize the population of Grey Wolves following their fitness

   Improve the chaotic number utilizing chaotic map equation

For every search agent

Improve the location of Current wolf utilizing equation 36

End for

Improve the parameters a, A, C

Determine the fitness of all wolves

Improve X_α, $X_{\beta, and}$ X_δ

Modify the worst fit wolf with the best fit wolf

t=t+1

End while

Return X_α

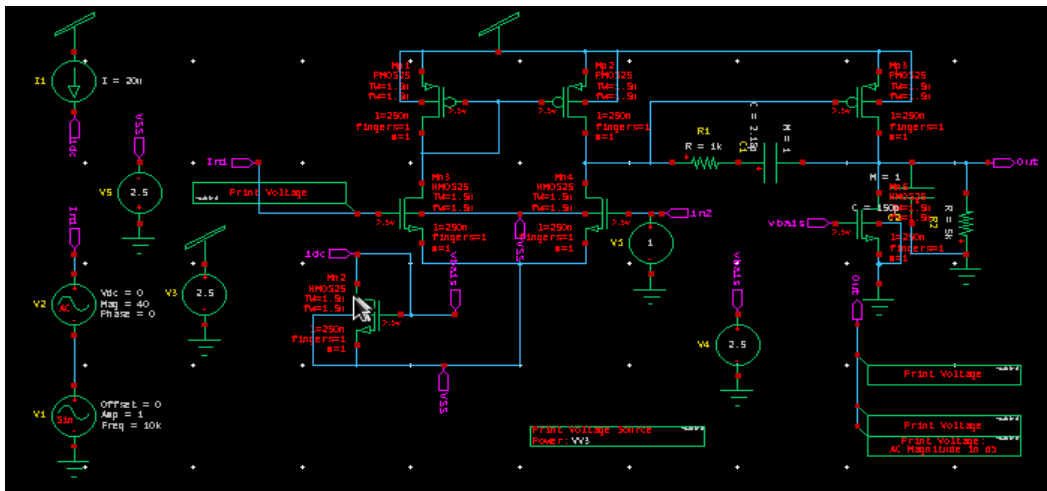Fig 3.   Algorithm of Proposed CGWO.

Fig 4.   Schematic of the Proposed Two Stage CMOS Operational Amplifier.
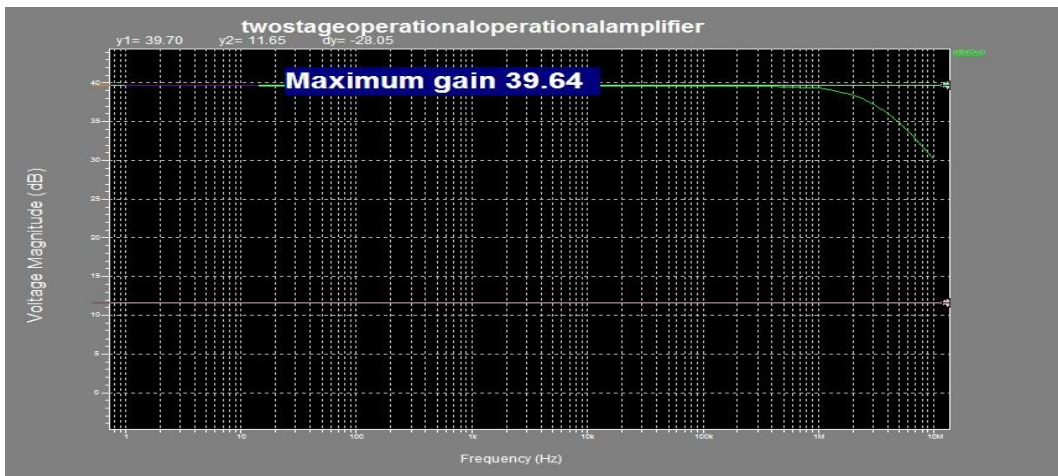

Fig 5.   Gain of the Proposed Two Stage CMOS Operational Amplifier.

Fig 6.   Power Dissipation of the Proposed Two Stage CMOS Operational Amplifier (72uw).

Table III contains Technology parameters, inputs and lengths of MOS transistors and Table IV. contains the values for the parameters attained for diverse techniques applied for the proposed circuit. Table V. Presents the values for the specifications attained by the diverse techniques employed for the proposed circuit.

TABLE III.   TECHNOLOGY PARAMETERS, INPUTS, AND LENGTH OF MOS TRANSISTORS

S.No	Specification	Values used
1	$V_{DD}(V)$	2.5
2	V_{SS} (V)	-2.5
3	$V_{tP}(V)$	-0.39
4	Vtn(V)	0.35
5	$K'_{N'}(\mu A/V^2)$	177.2
6	$K'_P(\mu A/V^2)$	35.6
7	Length (μm)	0.18

TABLE IV.   VALUES FOR THE PARAMETERS ATTAINED FOR DIVERSE TECHNIQUES FOR THE PROPOSED CIRCUIT

Design Parameters	CGWO	GA	DE
$I_{BIAS}(\mu A)$	22.2	34.5	42
C_c	2.18 pf	2.43 pf	2.47 pf
W_1/L_1	8=1.44/0.18	2/0.18	4/0.18
W_2/L_2	8=1.44/0.18	2/0.18	4/0.18
W_3/L_3	4=0.72/.18	4/018	4/0.18
W_4/L_4	4=0.72/0.18	4/0.18	4/0.18
W_5/L_5	1=0.4/0.4	2/0.18	4/0.18
W_6/L_6	40=7.20/0.18	22.64/0.18	24.86/0.18
W_7/L_7	8=1.44/0.18	8/0.18	8.2/0.18

The CMRR can be computed as $CMRR = 20 \, LOG_{10} \, \frac{A_{v\,DIFF}}{A_{v\,COMM}}$

The PSRR can be computed as $PSRR = 20 \, LOG_{10} \, \frac{A_{v\,DIFF}}{A_{v\,PS}}$

TABLE V.   VALUES FOR THE SPECIFICATIONS ATTAINED BY THE DIVERSE TECHNIQUES FOR THE PROPOSED CIRCUIT

Design Criteria	Specifications	CGWO	GA	DE
Slew Rate (V/ μs	≥ 10 V / μs	20	15	10
Load Capacitance C_L(pf)	≥ 10 pf	12	9	7
Gain in dB	40 dB	39.64	36.48	32.42
Unity Gain Bandwidth MHz	≥ 5 MHZ	18.43	16.54	12.14
$VI_{c\,(min)}$	≥ -1.5v	-0.01	-0.2	-1.2
$VI_{c\,(max)}$	≤ 2V	1.10	1.01	1.05
Power Dissipation P_{diss} (μw)	≤ 2000 μ watt	72	117	147.2
Total Area	≤ 300 μm^2	71.26	94.7	107.845
Phase Margin in Degree	≥ 60 Degree	58.6	48.4	42.7
CMRR	≥ 60 dB	134.6	133.7	132.7
PSRR	≥ 60 dB	180	179.1	178.2

VI. CONCLUSION

The motivation of this paper is to optimize the power dissipation in the design of a circuit with compact size and low power operational amplifier. For the design of two-step CMOS-OPAMP, a thoroughly explained strategy is presented in the paper. It is observed that the power dissipation accomplished with the CGWO technique performed superior to the genetic algorithm and differential evolution also attained the best convergence rate and duration complexity by analyzing the results with the above-mentioned algorithms. The designed circuit can offer a reasonable gain for open-loop configurations. On the other hand, the issue in the circumstance is the steadiness that might be diminished by utilizing the compensation procedures. The circuit selected employs the Miller Compensation methodology, in such a way that modest frequency compensation practice utilizes the Miller impact by joining a compensation capacitor in parallel to the high-gain phase. It is clearly explained from the achieved results that, utilizing CGWO as an optimization technique can minimize the current, power consumption and area as well.

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