PHY-DTR: An Efficient PHY based Digital Transceiver for Body Coupled Communication using IEEE 802.3 on FPGA Platform

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***Abstract*—Body coupled communication (BCC) is an efficient networking approach to body area network (BAN) based on Human-centric communication. The BCC provides interference only between humans in very close proximity. In this work, an efficient Physical layer (PHY) based digital transceiver) is designed for BCC. The digital transceiver Module mainly contains a Digital transmitter (TX) with Manchester encoder, clock synchronization unit, and Digital receiver (RX) with Manchester decoder. The TX and RX modules are designed using a finite state machine as per the IEEE 802.3 Standards. The complete work is also varied for BAN applications by connecting two Application layer transceivers and two Physical layer-based digital transceivers. The architecture is simulated in a Model-sim simulator. The complete Module is synthesized using different FPGA families, and the hardware design constraints are contrasted. The digital transceiver works at 231.28 MHz operating frequency, consumes 0.113W power, and provides a 7.7 Mbps data rate and 4.67 Kbps/Slice efficiency on Artix-7 FPGA. The proposed transceiver is also compared with existing digital transceivers with hardware constraints improvements.**

***Keywords*—Body coupled communication; physical layer; digital; FPGA; radiofrequency; human body**

I. INTRODUCTION

The body area network technology with wireless connectivity is one of the promising technologies in the Health care domain because of its flexibility and portability. The BAN visualizes and controls the operating sensors, which can measure the critical physiological and physical parameters. Radiofrequency (RF) based wireless technology is deployed in BAN systems, which lag battery power, security, and electromagnetic issues [1]. Intra body-communication (IBC) is an alternative non-RF technology, which uses the human body as a transmission medium for signals (electrical) and overcomes most of the RF-technology-related issues [1-2]. The IBC gives lower power and better data rates; this results in an alternative to short-range communications. The IBC has different types, each having unique properties. The well-suited wireless communications types are Ultrasound (US), galvanic coupling, resonant coupling, and capacitive coupling [3-4]. There are many electrical coupling techniques available for data transmission through the human body. In general, electromagnetic wave and electrostatic coupling are the two commonly used transmission methods in IBC. The IBC is used in many applications like touching voice system, blind person assistance system, speech assistance for dumb persons [5]. The wireless BAN comprises mainly three PHY schemes: Narrowband (NB), ultra-wideband (UWB), and Human body communication (HBC) as per IEEE 802.15.6 standardization [6]. The NB and UWB schemes are related to RF technologies, whereas HBC is related to Non-RF technologies. The HBC is also considered body channel communication and body coupled communications in the current work [7]. The human body is used as a signal transmission medium in BCC, connected with electronic devices nearby, to provide human-centric communication. The BCC transceiver [8-9] is designed to achieve better power efficiency and data rates by avoiding the fading effects. The Overview of the BCC transceiver architecture is represented in Fig. 1. It mainly contains BCC TX and RX modules. The BCC-TX mainly has three parts: Application layer, PHY-based digital TX, and Analog front-end (AFE) part. Similarly, BCC-RX has an AFE part, followed by a PHY-based digital RX and application layer.

The Digital Transmitter receives data from the application layer (AL) and converts it into a packet sent using unified communication over the human body. These packets are processed further in the AFE part of the transmitter. The Digital receiver collects the data serially from the AFE receiver part and recovery the data with proper operation in DR. It sends it back to the application layer. The complete PHY-based D-TR is working in full-duplex communication mode for BCC. The application layer collects data from the user on the transmitter side and displays its output. The Ethernet protocol is used in PHY as per IEEE 802.3 standards for transmitting and receiving BCC transceiver data. The Manchester encoding and decoding modulation techniques are incorporated in the transceiver, which is used significantly in the human body with capacity coupling. The transmission line or capacitive approaches are used as a coupling mechanism, interconnecting BCC TX and BCC RX of the Human body. There is always a challenge to design communication protocols for BCC by analyzing each layer's -fundamental features like the application layer, Media Access Control (MAC) layer, and physical layer. The MAC layer supports the IEEE 802.3 ethernet Protocol, which provides a high data rate, and more influenced for real-time application cases for the BBC system.

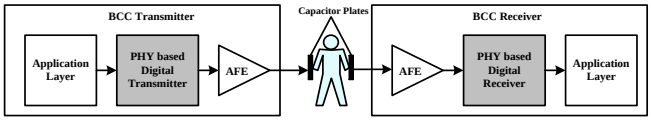


Fig. 1. BCC Transceiver Architecture Overview.

The PHY-based digital transceiver architecture is designed for BCC and Prototyped on the FPGA platform in this work. The proposed transceiver provides effective data rates and that can be used for Human Body. The rest of the paper is organized as Section II explains the existing BCC works and its transceiver modules using different design parameters. The proposed PHY-based digital Transceiver architecture is explained in detail in Section III. Section IV discusses the different design constraints of PHY-based digital transceivers on different FPGA families. Finally, Section V concludes the overall work of the PHY-based digital transceiver and suggests the future scope.

II. Related Work

In this section, the review of the existing body coupled communication architectures is done. Arenas et al. [10] present the BCC module for streaming music using Universal software Radio peripheral (USRP) hardware module and GNU radio. The signal generator is used to measure the body channel frequency and its response. The obtained 128 kbps data rate is verified using a Vector network analyzer (VNA). Achieving a higher data rate is noted to be difficult in this work. Yoo et al. [11] discuss the energy-efficient BCC for Body area network applications. The work analyses the space, time concerning channel gain, environmental variation, power consumption details, and benefits. The work uses a pseudo OFDM transceiver module, which consumes more chip area and power in real-time implementations. Kado et al. [12] present the embedded transceiver architecture for the human body. The work is based on near field coupling architecture using human Area networks (HAN). The work discusses the better packet error rates (PER) by concerning the received signal power for uplink and downlink transmission. The embedded transceiver achieves minimal data rate and consumes more power for received packets. Matias et al. [13] discuss the Capacitive BCC via the ECG acquisition system. This work elaborates on capacitive coupling with the BCC transceiver system connected to the ECG monitoring system. It analyses the received ECG signal with a 100kbps data rate on the mobile device. The designed BCC system is suitable only for ECG monitoring applications and not applicable for HBC. Takeuchi et al. [14] present the wearable Near-field coupling (NFC) Transceiver architecture using handshaking communication. The battery-powered TR with a digital synthesizer is an equivalent circuit for handshaking communication between two humans. The results of signal propagation loss and received voltage concerning two human bodies are analyzed. The work is suitable only if humans were 600-800 mm apart and is reported to be not suitable for higher ranges.

Saadeh et al. [15-16] implement the BCC TR for Binaural hearing aids for BAN. This work uses Pseudo OFDM TR with Frequency shifting keying schemes for BCC TR to improve TR's Bit error rate at a 1 Mbps data rate. The traditional Pseudo OFDM TR consumes more chip area and power and not suitable for real-time HBC. Zhao et al. [17] present Human Body communication TR compatible with IEEE 802.15.6 and achieves less BER and 5.25 Mc/s chip rate. The mask-shaped transmitter and digital controlled calibration-based receiver are designed for HBC TR. The designed work is intricate and consumes more area on the 65nm- CMOS chip process. Chung et al. [18] implement the BCC TR using Walsh codes on the FPGA platform for HBC. The jitter tolerance and code rate are improved using Walsh codes. The BCC TR achieves the 10-8 BER at a 6.25 Mcps data rate. The implemented BCC TR uses only Walsh code-based data transmission without using MAC features.

Park et al. [19] discuss the Magnetic HBC TR by enabling 5Mbps data at 40MHz carrier frequency. This work discusses the design challenges of different HB TR modulation and demodulation schemes. The results are obtained on the ASIC Platform and analyze the data rate and power consumption. The data rate can be further improved by using a suitable modulation scheme. Muzaffar et al. [20] present the BCC TR, which provides low-power, self-synchronization, and low complexity while implementing on the human body. The TR is verified on the oscilloscope for received and transmitted signals through the body. The work also analyses the energy and power consumption of BCC TR with an average data rate of 21Mbps at 125MHz. Krhac et al. [21] present the HBC channel analysis on the simulation platform, which provides a forward transmission coefficient for various capacitive return paths and electrode distances. The work is analyzed in the software environment and not compactable to real-time HBC. Jeon et al. [22] discuss the BCC TR for Bionic arms using a galvanic coupling. The BCC TR is designed using CMOS 0.18 µm, which provides better energy efficiencies of 4.75 pJ/b and 26.8pJ/b for TX and RX, respectively, and improves the 10-8 BER using a galvanic coupling at 100Mbps data rate. Yoo et al. [23] present the BAN TR using BCC, which provides a better energy-efficient TR communication system. The conventional pseudo –OFDM-based BCC TR is designed for BAN, which offers a 1Mbps data rate.

Wei et al. [24] present the intra-body communication (IBC) TR with galvanic coupling (GC) using differential phase shifting keying (DPSK) schemes. This work achieves a 1Mbps data rate with 0.6mA of coupling amplitude. The data acquisition module is designed in a Lab-view environment, and TR is designed on FPGA, which consumes more chip area. Chen et al. [25] discuss the GC-based IBC TR using Direct sequence spread spectrum (DS-SS) Technology. The DSSS-DPSK based TR achieves better BER and SNR than DPSK based TR. The designed TR is complex and works at a 50kbps data rate, and will not effective in WBAN. Botero et al. [26] review the HBC channel characteristics' issues using different coupling techniques with different measurement approaches. Slot et al. [27] present the heartbeat-based MAC architecture for BCC applications. The TDMA based MAC protocol is introduced for packet transmission and reception in capacitive BCC architecture for heartbeat sensing. Ormanis et al. [28] discuss human body frequency response as a case study in BCC for e-Health. The human body frequency

response range is up to 30MHz using BCC. Li et al. [29] present the Differential AFE receiver for Galvanic-coupled HBC. The Stability of AFE in the frequency range is up to 1MHz, and AFE reduces the interference margin to a great extent. Vizziello et al. [30] present PHY implementation for IBC links using a galvanic coupling. The Galvanic coupling method analyses the selection of modulation schemes, frequency parameters, and recovery of baseband signals.

It has been noticed from the above existing work that most of the BCC transceivers are entirely designed on software and very few on FPGA and ASIC Platform. Significantly less work on the PHY-based digital transceiver with MAC features support for BCC system. There remains a scope to develop schemes to achieve higher data rates with novel transceiver architecture designs. In this proposed work, an efficient PHY-based digital DTR is designed to overcome data rate limitations.

III. PHY BASED DIGITAL TRANSCEIVER

The physical layer-based D-TR is designed for BCC and is detailed in this section. The IEEE 802.3 Ethernet protocol standard is adopted for transmitting and receiving the packets in PHY-based D-TR. The IEEE 802.3 Ethernet protocol supports the 10Mbps data rate with the baseband signaling method, and the co-axial medium is selected in PHY. The PHY-based D-TR module contains a digital transmitter, digital receiver, Manchester encoder and decoder, and clock synchronization module (CSM), as represented in Fig. 2. The PHY-based digital TR sub-modules are explained in the sub-sections next.

A. Digital Transmitter (D-TX)

The AL provides the data information to the D-TX and proceeds with Manchester encoded data serially in the transmitter's AFE part. The D-TX mainly contains two memory modules-one for preamble generation and another for data storage. The D-TX has a Packet framing unit (PFU), shift register, Frame check sequence (FCS) unit, Transmitter-FSM for controlling the D-TX, and Manchester encoder. The D-TX clock frequency is set at 100MHZ. The D-TX receives the data from the application layer, temporarily stores the data in memory, and assembles the packet form data. It is represented in Fig. 3. The preamble generation information is stored in memory 1 (MEM1). The MEM1 holds eight 8-bit preamble values and is used for clock synchronization with PHY. The Packet framing unit processes the application layer data as per the IEEE 802.3 standard.

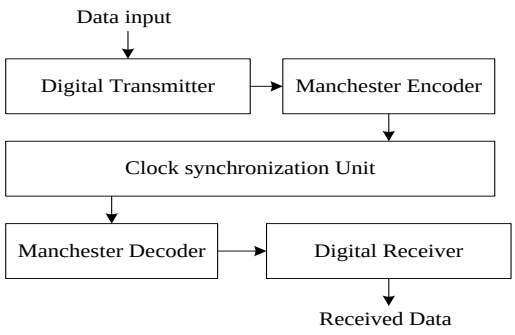


Fig. 2. PHY based Digital Transceiver (D-TR) Architecture.

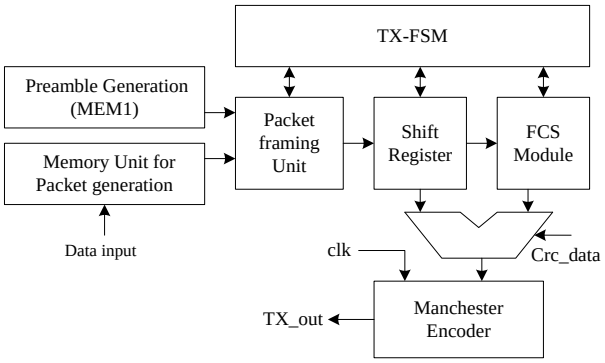


Fig. 3. PHY based Digital Transmitter Architecture.

The IEEE 802.3 Packet format for Ethernet protocol is represented in Fig. 4. The Packet format starts with a preamble, followed by the frame (SOF) Delimiter, Length field, Source and destination ID, payload data, and Frame check sequence.

The 7-bytes preamble is used to synchronize the clock with the physical layer and intimates incoming frames to the receiver station. The SOF delimited initiates the first-byte frame data. The 2-6 bytes of Source and destination ID contains address information of transmitting and receiving station, respectively. The 2-byte length field provides payload (data) information. The 46-1500 bytes of the payload can be accessed in the Ethernet frame. The 2-4 bytes of frame check sequence provides error detection features using cyclic redundancy check (CRC). In the D-TX module, 7-Bytes of Preamble, 1-byte of SOF delimiter, 1-byte of source and destination ID, 2-bytes of length, 64-bytes of payload data, and 2-bytes of FCS data is considered.

The transmitter-FSM is mainly used to control switching activity between the different fields and provides proper communication. The detailed TX-FSM is represented in Fig. 5.

7-bytes	1-byte	2-6 bytes	2-6 bytes	2-bytes	46-1500 bytes	2-4 bytes
Preamble	SOF	Destination ID	Source ID	Length	Payload	FCS

Fig. 4. Standard IEEE 802.3 Packet format (Ethernet).

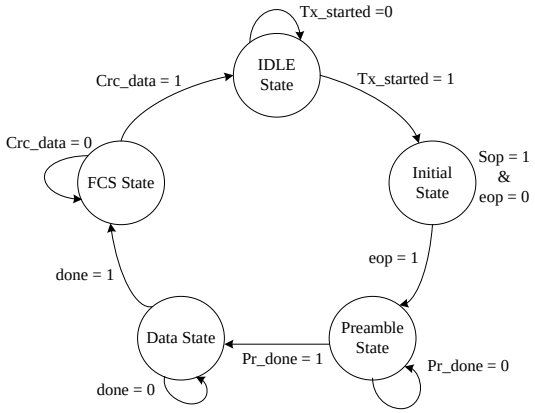


Fig. 5. Transmitter-FSM Diagram.

The five states are used in FSM, IDLE state, Initial state, Preamble state, data state, and FCS state. In the IDLE state, the transmission process (TX started) is started when RX is not busy. The initial state provides first Packet data by providing two handshaking signals (start of packet (sop) =1 and end of packet (eop) =0) from the PHY medium. When eop is activated, the preamble state sends the preamble data by activating Pr_done=1 to the data state. In the data state, the input data receiving from the memory unit and activates the done signal. In the FCS state, the CRC is used to check the packets' status, like packet data is valid or not; the packet is short or long; any error occurs in the packet or not. The CRC has also detected errors and validate the packet. The shift register is used to generate the serial data by shifting 1-bit left using a framed packet. The FCS module receives the serial data and checks the error status using CRC. If the CRC data is activated, the FCS data else shift register's serial data is used in the Manchester encoder. The CRC is modeled using a linear feedback shift register (LFSR). The 16-bit LFSR polynomial is used for error detection for the given packet. The 16-bit LFSR polynomial for CRC module is expressed as: 1 + x4 + x11+ x15. The Manchester encoder provides better baseband modulation to the D-TX module.

The clock signal is XOR with serial data for the generation Manchester encoded data (Tx_data) as a D-TX output. The Encoded data is in the form of '0' or '1'. The transition occurs either from '0' to '1' and from '1' to '0' in every clock cycle. In further, these encoded data are used in the clock synchronization unit to recover the clock.

B. Clock Synchronization Unit

The clock synchronization unit receives the encoded data serially in an oversampling manner. The clock synchronization unit uses the clock signal 8 times faster than the D-TX clock signal. This clock signal provides the transition edges by using the receiving the data signal. If the Manchester encoded data is one, the clock detects it as a positive edge; otherwise, it is a negative edge. The combination of positive and negative edges detects the recovered clock when similar data bits match. If the received data is not matched, then the central transition signal is activated, with the clock signal's absence in the received data. The recovered clock is oversampled with received data for the formation of the decoded output. The Manchester decoder uses X-NOR operation to decodes the received data with the recovered clock. The decoded data is used as a serial input to the D-RX module.

C. Digital Receiver

The PHY-based Digital Receiver Architecture and The RX-FSM are represented in Fig. 6 and Fig. 7, respectively. The D-RX mainly contains a Delay unit, Preamble checking unit, SOF finding unit, length activation unit, packet recovery unit, matching unit, Memory unit, and RX-FSM. The D-RX receives the Manchester decoded data and input it into the delay unit. The delay unit contains many data flip-flops (D-FF), which synchronize the decoded data for proper packet recovery. The RX-FSM is used to control all the submodules with proper interconnection signals.

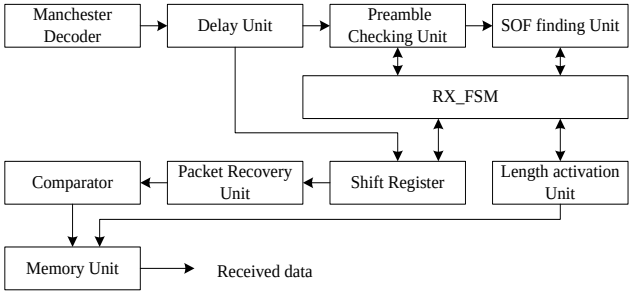


Fig. 6. PHY based Digital Receiver Architecture.

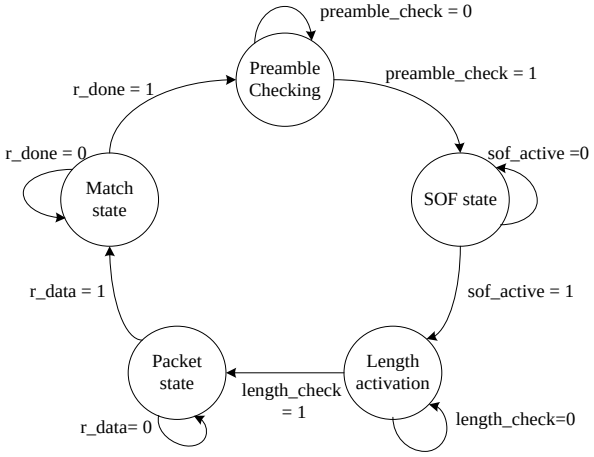


Fig. 7. Receiver-FSM Diagram.

The RX-FSM mainly contains five states, namely: Preamble checking state, SOF state, length activation state, packet recovery state, match state. The Preamble checking state checks the first 16-bits of the data; if it matches, then move to the SOF delimiter state. In SOF State, the two successive '1' appear, then the state transitions to the Length activation state. Decode the first two bytes of the data using a shift register and delay unit to check the packet's length and store these two bytes of the packet length in the Memory unit. The packet state recovers the data packet after the recovery of the complete data from the delay unit. The match state checks the source ID with the next consecutive of the recovered packet, if it matches, the recovery operation is completed, and signal r_done is activated. The D-RX Module Stop receiving data from the clock synchronization unit. The recovered data stored in memory to validate the received and transmitted data packets are not. If the recovered packets are not matched, then the same process repeats until valid packets are recovered.

The designed PHY-based digital transceiver is verified for Body area network applications, represented in Fig. 8. Two Application layer transceivers (AL-TR1 and AL-TR2) and Two PHY-based digital transceivers are used for verification. The AL-TR1 received the data (Tx) from the user, passed to the PHY-TR1, and received the output data (Rx) from PHY-TR1. Similarly, The AL-TR2 received the data (Tx) from the user, passed to the PHY-TR2, and received the output data (Rx) from PHY-TR2. The standard clock signal is used for two PHY-TR, which is received from the AL-TR. The clock

signal frequency may vary upon application usage. For example, when the PHY-TR1 wants to send the data to PHY-TR2, it first checks the availability of PHY-TR2. If it is ready, the data is sent to the PHY-TR2, which decodes the data packet until the destination ID matches and processes further to the AL-TR-2.

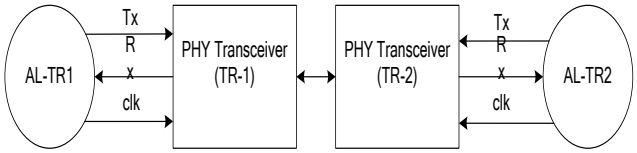


Fig. 8. PHY-Transceiver Verification overview for BAN Application.

IV. Results and Discussion

The results of the PHY-based digital transceiver are discussed in this section. The Complete architecture is designed using VHDL on the Xilinx ISE environment and simulated using a Modelsim simulator. The PHY-based digital transceiver module is implemented and prototyped using Artix-7 FPGA (XC7A100T-3CSG324). The PHY-based digital transceiver submodules design constraints are tabulated in Table I. The Digital TX utilizes 750 slices, works at 297.38 MHz, and consumes 0.088W total power.

Similarly, the clock synchronization (Clock_Sync) unit utilizes 45 slices, works at 352.78 MHz, and consumes 0.104W total power. The clock synchronization module uses an 800MHz clock frequency, which is 8-times faster than the Digital TX clock frequency. The Digital RX utilizes 696 slices, works at 219.13 MHz, and consumes 0.090W total power.

The Performance parameters for PHY-based Digital transceivers using different FPGA families like Spartan-6, Artix-7, and Viretx-7 are tabulated in Table II. The Spartan-6 FPGA uses 45-Nm CMOS Technology, whereas Artix-7 and Virtex-7 use 28nm CMOS Technology. The PHY-based D-TR utilizes 1672 slices, 2586 LUT's, works at 145.21 MHz, and consumes 0.092W total power on Spartan-6 FPGA. Similarly, The PHY-based D-TR utilizes 1646 slices, 2517 LUT's, works at 231.28 MHz, and consumes 0.113W total power on Artix-7 FPGA. The PHY-based D-TR utilizes 1646 slices, 2518 LUT's, works at 310.01 MHz, and consumes 0.22W total power on Virtex-7 FPGA.

The PHY-based Digital Transceiver latency is calculated based on the simulation results obtained using the Modelsim simulator. The PHY-based Digital Transceiver takes 240 clock cycles (CC) to receive the first packet data. The period of one clock cycle is defined as 16 ns. The PHY-based Digital Transceiver throughput is calculated using latency (CC), the number of input data passed, and the design's maximum operating frequency. So, throughput (Mbps) = (Input data * Max. frequency)/latency. Only 7 input packets are considered for simulation purposes. The throughput (data rate) of 4.84Mbps, 7.7Mbps, and 10.33Mbps obtained on Spartan-6, Artix-7, and Virtex-7 FPGA families PHY-based Digital Transceiver. The *Throughput of 3.33 Mbps is obtained for Maximum operating frequency 100MHz, a suitable BCC Transceiver [9] Module. The Hardware efficiency is calculated based on Throughput per slice (Kbps/Slice). The Hardware efficiency of 2.89 Kbps/Slice, 4.67 Kbps/Slice, and 6.27 Kbps/Slice was obtained for Spartan-6, Artix-7 Virtex-7 FPGA families, respectively.

The Chip Area utilized for PHY-based Digital Transceiver on different FPGA families like Spartan-6, Artix-7, and Viretx-7 are represented in Fig. 9(a), 9(b), and 9(c), respectively. The Chip Area Utilization on different FPGAs is obtained after the place and route operation using the Xilinx FPGA editor Tool.

TABLE I. Resources utilized for PHY based Digital Transceiver Sub-Modules on Artix-7 FPGA

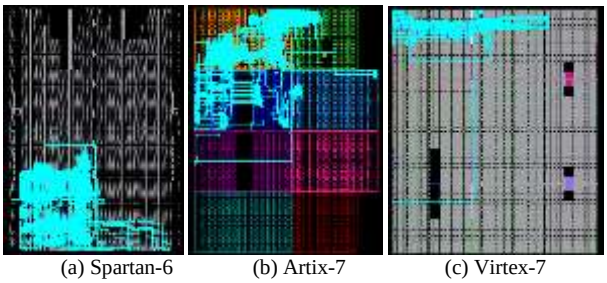
Resource Used	Digital TX	Clcok_Sync Unit	Digital RX
Slice Registers	750	45	696
Slice LUTs	760	99	1129
LUT-FF pairs	230	43	662
Minimum Period (ns)	3.363	2.835	4.563
Max.Frequency (MHz)	297.38	352.787	219.13
Total Power (W)	0.088	0.104*	0.09

*800 MHz clock Frequency (which is 8 times faster than TX clock frequency)

TABLE II. Performance Parameters for PHY based Digital Transceiver using different FPGA's

Resource Used	PHY based Digital Transceiver on Different FPGA Families		
FPGA Family	Spartan-6	Artix-7	Virtex-7
FPGA Device	XC6SLX45T-3CSG324	XC7A100T-3CSG324	XC7V330T-3FFG1157
CMOS Technology	45nm	28nm	28nm
Slices	1672	1646	1646
LUTs	2586	2517	2518
Max. Frequency (MHz)	145.214	231.28	310.017
Total Power (W)	0.092	0.113	0.22
Latency (Clock cycles)	240	240	240
Throughput (Mbps)	4.84	7.7	10.33
*Throughput (Mbps)	3.33	3.33	3.33
Efficiency (Kbps/Slice)	2.89	4.67	6.27
*Efficiency (Kbps/Slice)	1.91	2.02	2.02

*100 MHz Operating Frequency suitable for BCC [9]



(a) Spartan-6 (b) Artix-7 (c) Virtex-7

Fig. 9. Chip Area utilized for PHY based Digital Transceiver on different FPGA.

The comparison results of different PHY based Digital Transceiver's on hardware platform is tabulated in Table III. For the comparison, different hardware constraints like the selection of FPGA device, Slice, LUT's Power (mW), and throughput (Mbps) are considered. The baseband transceiver [31] is implemented on spartan -6 FPGA for BAN communication. The work utilizes 2843 slice registers, 3915 LUT's, consumes 192mW power, and works at 0.187Mbps. The Proposed digital transceiver is compared with the existing transceiver [31], with an improvement in overhead for 41.18% in slices, 33.94% in LUT's and 52% in power utilization. The physical transceiver [32] is designed on Virtex-6 FPGA for WBAN applications, which utilizes 2668 slice registers, 3161 LUT's, consumes 117mW power, and works at 0.121 Mbps. The Proposed digital transceiver is compared with the existing PHY transceiver [32], with an improvement in overhead for 37.33% in slices, 18.19% in LUT's and 21.3% in power utilization. The proposed PHY-based digital transceiver provides better throughput than the other two compared transceivers.

The proposed digital transceiver is designed, and it is optimized with the help of FSM's. The proper data packets transmission and reception are achieved using TX and RX-FSM's with a clock synchronization mechanism. The FSM is activated only when necessary or in the initial state while transmission/ reception of data packets.

TABLE III. COMPARISON RESULTS OF DIFFERENT PHY BASED DIGITAL TRANSCEIVER'S

Resources	**Ref [31]**	**Ref [32]**	**Proposed**
FPGA	Spartan-6	Virtex-6	Spartan -6
Slices	2843	2668	1672
LUT's	3915	3161	2586
Power (mW)	192	117	92
Throughput (Mbps)	0.187	0.121	4.84

V. CONCLUSION

In this paper, an efficient PHY-based D-TR is designed for BCC. The PHY-based D-TR receives or transit the packets to and from the application layer and supports full-duplex combination using 802.3 IEEE communication protocol standards. The PHY-based D-TR incorporates Manchester encoding-decoding mechanism to recover the complete data packet with proper clock synchronization. The architecture utilizes 1% slices, 3% LUT's, works at 231.28 MHz maximum frequency, and consumes a total power of 0.113W on Artix-7 FPGA. The architecture works at 7.7 Mbps throughput with an efficiency of 4.67 kbps/slice on Artix-7 FPGA. The PHY-based Digital Transceiver synthesized on different FPGA families like Spartan-6, Artix-7, and Virtex-7 and obtained different design constraint results. The PHY-based D-TR obtains a throughput of 3.33Mbps at 100 MHz, suitable for the BCC [9] system. In the future, the design of a complete BCC transceiver using the proposed PHY-based digital transceiver design of Human body communication transceiver can be modeled as per 802.15.6 IEEE standard for BAN applications.

REFERENCES

[1] Seyedi, M., Kibret, B., Lai, D. T., & Faulkner, M. (2013). A survey on intrabody communications for body area network applications. IEEE Transactions on Biomedical Engineering, 60(8), 2067-2079.

[2] Zhao, J. F., Chen, X. M., Liang, B. D., & Chen, Q. X. (2017). A review on human body communication: signal propagation model, communication performance, and experimental Issues. Wireless Communications and Mobile Computing, 2017.

[3] Tomlinson, W. J., Banou, S., Yu, C., Stojanovic, M., & Chowdhury, K. R. (2018). A comprehensive survey of galvanic coupling and alternative intra-body communication technologies. IEEE Communications Surveys & Tutorials, 21(2), 1145-1164.

[4] Corroy, S., Argyriou, A., Bhatti, Z. W., & Baldus, H. (2010). A body-coupled communication and radio frequency dual technology cooperation protocol for body area networks. In ICC'10 Workshop on Medical Applications Networking, Date: 2010/05/27-2010/05/27, Location: Cape Town, SA. IEEE.

[5] Shimamoto, S., Alsehab, A. M., Kobayashi, N., Dovchinbazar, D., & Ruiz, J. A. (2007, December). Future applications of body area communications. In 2007 6th International Conference on Information, Communications & Signal Processing (pp. 1-5). IEEE.

[6] Astrin, A. (2012). IEEE standard for local and metropolitan area networks part 15.6: Wireless body area networks. IE EE Std 802.15. 6.

[7] Song, S. J., Cho, N., Kim, S., Yoo, J., Choi, S., & Yoo, H. J. (2007, February). A 0.9 V 2.6 mW body-coupled scalable PHY transceiver for body sensor applications. In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (pp. 366-609). IEEE.

[8] Fazzi, A., Ouzounov, S., & van den Homberg, J. (2009, February). A 2.75 mW wideband correlation-based transceiver for body-coupled communication. In 2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers (pp. 204-205). IEEE.

[9] Baldus, H., Corroy, S., Fazzi, A., Klabunde, K., & Schenk, T. (2009). Human-centric connectivity enabled by body-coupled communications. IEEE Communications Magazine, 47(6), 172-178.

[10] Arenas, G. M., & Gordillo, A. C. (2016, October). Design and implementation of a body-coupled communication system for streaming music. In 2016 IEEE ANDESCON (pp. 1-4). IEEE.

[11] Yoo, J. (2017). Body coupled communication: Towards energy-efficient body area network applications. In 2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) (pp. 244-246). IEEE.

[12] Kado, Y., Kobase, T., Yanagawa, T., Kusunoki, T., Takahashi, M., Nagai, R & Shinagawa, M. (2012, January). Human-area networking technology based on near-field coupling transceiver. In 2012 IEEE Radio and Wireless Symposium (pp. 119-122). IEEE.

[13] Matias, R., Cunha, B., Mota, A., & Martins, R. (2014, June). ECG monitoring via Capacitive Body Coupled Communications. In 2014 IEEE International Symposium on Medical Measurements and Applications (MeMeA) (pp. 1-6). IEEE.

[14] Takeuchi, R., Hasegawa, S., Kado, Y., Ayuzawa, D., Shinagawa, M., Ohashi, K., & Saito, D. (2017, March). Implementation methodology of handshaking communication using wearable near-field coupling transceivers. In 2017 11th European Conference on Antennas and Propagation (EUCAP) (pp. 1871-1875). IEEE.

[15] Saadeh, W., Altaf, M. A. B., Alsuradi, H., & Yoo, J. (2017). A pseudo OFDM with miniaturized FSK demodulation body-coupled communication transceiver for binaural hearing aids in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 52(3), 757-768.

[16] Saadeh, W., Altaf, M. A. B., Alsuradi, H., & Yoo, J. (2017). A 1.1-mW ground effect-resilient body-coupled communication transceiver with pseudo OFDM for head and body area network. IEEE Journal of Solid-State Circuits, 52(10), 2690-2702.

[17] Zhao, B., Lian, Y., Niknejad, A. M., & Heng, C. H. (2018). A low-power compact IEEE 802.15. 6 compatible human body communication transceiver with digital sigma-delta IIR mask shaping. IEEE Journal of Solid-State Circuits, 54(2), 346-357.

[18] Chung, C. C., Chang, R. H., & Li, M. H. (2018, May). An FPGA-Based Transceiver for Human Body Channel Communication Using Walsh

Codes. In 2018 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW) (pp. 1-2). IEEE.

[19] Park, J., & Mercier, P. P. (2019). A Sub-10-PJ/bit 5-Mb/s Magnetic Human Body Communication Transceiver. IEEE Journal of Solid-State Circuits, 54(11), 3031-3042.

[20] Muzaffar, S., & Elfadel, I. M. (2019, July). A Self-Synchronizing, Low-Power, Low-Complexity Transceiver for Body-Coupled Communication. In 2019 41st Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC) (pp. 4036-4039). IEEE.

[21] Krhac, K., Sayrafian, K., Noetscher, G., & Simunic, D. (2019, July). A Simulation Platform to Study the Human Body Communication Channel. In 2019 41st Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC) (pp. 4040-4043). IEEE.

[22] Jeon, Y., Jung, C., Cheon, S. I., Cho, H., Suh, J. H., Jeon, H., & Je, M. (2019, June). A 100Mb/s Galvanically-Coupled Body-Channel-Communication Transceiver with 4.75 pJ/b TX and 26.8 pJ/b RX for Bionic Arms. In 2019 Symposium on VLSI Circuits (pp. C292-C293). IEEE.

[23] Yoo, J. (2019). Energy-Efficient Body Area Network Transceiver Using Body-Coupled Communication. In The IoT Physical Layer (pp. 127-139). Springer, Cham.

[24] Wei, Z. L., Chen, W. K., Yang, M. J., Gao, Y. M., Vasić, Ž. L., & Cifrek, M. (2020, May). Design and Implementation of Galvanic Coupling Intra-Body Communication Transceivers using Differential Phase Shift Keying. In 2020 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) (pp. 1-6). IEEE.

[25] Chen, W. K., Wei, Z. L., Gao, Y. M., Vasić, Ž. L., Cifrek, M., Vai, M. I & Pun, S. H. (2020). Design of Galvanic Coupling Intra-Body Communication Transceiver Using Direct Sequence Spread Spectrum Technology. IEEE Access, 8, (pp 84123-84133).IEEE.

[26] Álvarez-Botero, G. A., Hernández-Gómez, Y. K., Telléz, C. E., & Coronel, J. F. (2019). Human body communication: Channel characterization issues. IEEE Instrumentation & Measurement Magazine, 22(5), (pp. 48-53).

[27] Solt, F., Benarrouch, R., Tochou, G., Facklam, O., Frappé, A., Cathelin, A & Rabaey, J. M. (2020). Energy Efficient Heartbeat-Based MAC Protocol for WBAN Employing Body Coupled Communication. IEEE Access, 8, 182966-182983.

[28] J. Ormanis and A. Elsts, (2020). Towards Body Coupled Communication for eHealth: Experimental Study of Human Body Frequency Response. In 2020 IEEE International Conference on Communications Workshops (ICC Workshops), Dublin, Ireland, (pp. 1-7). IEEE.

[29] Li, D., Wu, J., Gao, Y., Du, M., Vasić, Ž. L., & Cifrek, M. (2020, May). A Differential Analog Receiver Front-End for Galvanic-Coupled Human Body Communication. In 2020 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) (pp. 1-5). IEEE.

[30] Vizziello, A., Savazzi, P., Magenes, G., & Gamba, P. (2020). PHY Design and Implementation of a Galvanic Coupling Testbed for Intra-Body Communication Links. IEEE Access, 8, 184585-184597.

[31] Liang, Y., Zhou, Y., & Li, Y. (2014). The design and implementation of IEEE 802.15. 6 Baseband on FPGA. In The International Conference on Health Informatics (pp. 231-235). Springer, Cham.

[32] Mathew, P., Augustine, L., Kushwaha, D., Desalphine, V., & Selvakumar, A. D. (2015, January). Implementation of NB PHY transceiver of IEEE 802.15. 6 WBAN on FPGA. In 2015 International Conference on VLSI Systems, Architecture, Technology, and Applications (VLSI-SATA) (pp. 1-6). IEEE.