

# Failure Region Estimation of Linear Voltage Regulator using Model-based Virtual Sensing and Non-invasive Stability Measurement

Syukri Zamri, Mohd Hairi Mohd Zaman, Muhammad Fauzi Mohd Raihan  
Asraf Mohamed Moubark, M Marzuki Mustafa  
Department of Electrical, Electronic and Systems Engineering  
Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia  
43600 Bangi, Selangor, Malaysia

**Abstract**—Voltage regulator (VR) stability plays an essential role in ensuring maximum power delivery and long-lasting electronic lifespan. Capacitor with a specific equivalent series resistance (ESR) range is typically connected at the VR output terminal to compensate for instability of the VR due to sudden changes in load current. The stability of VR can be measured by analyzing output voltage during load transient tests. However, the optimum ESR range obtained from the ESR tunnel graph in its datasheet can only be characterized by testing a set of data points consisting of ESR and load currents. Characterization process is performed manually by changing the value of ESR and load current for each operating point. However, the inefficient process of estimating the critical value of ESR must be improved given that it requires a large amount of time and expertise. Furthermore, the stability analysis is currently conducted on the basis of the number of oscillation counts of VR output voltage signal. Therefore, a model-based virtual sensing approach that mainly focuses on black-box modeling through system identification method and training neural network on the basis of estimated transfer function coefficients is introduced in this study. The proposed approach is used to estimate the internal model of the VR and reduce the number of data points that need to be acquired. In addition, the VR stability is analyzed using noninvasive stability measurement method, which can measure phase margin from the frequency response of the VR circuit in closed-loop conditions. Results showed that the proposed method reduces the time it takes to produce an ESR tunnel graph by 84% with reasonable accuracy (MSE of  $5 \times 10^{-6}$ , RMSE of  $2.24 \times 10^{-3}$ , MAE of  $1 \times 10^{-3}$ , and  $R^2$  of 0.99). Therefore, efficiency and effectiveness of ESR characterization and stability analysis of the VR circuit is improved.

**Keywords**—Voltage regulator; output capacitor; equivalent series resistance; failure region; system identification; neural network; noninvasive stability measurement

## I. INTRODUCTION

Increasing demand for electronic products, such as system-on-chips and personal electronics, commonly requires the use of a voltage regulator (VR) for stable and regulated output voltage supply. VR has been widely used in the electronic field due to the development of new technologies and increasing demand for high-performance electronic devices and compact solutions [1],[2]. VRs in electronic devices are embedded in an integrated circuit (IC), but fault probability of the VR can be

influenced by a few parameters, such as temperature, input voltage supply, and aging factors [3],[5],[6]. These factors may further deteriorate internal parameters and thus reduce the performance of electronic devices or completely eliminate their functionality [21]. Therefore, industrial electronic manufacturers must perform stability analysis of the VR.

The existing analysis for VR stability through ESR and load is performed manually [4],[7]. This method is solely conducted by testing a vast number of data, observing load transient, and varying the load current for a specific ESR value. Thus, an accurate ESR tunnel graph can be obtained to show stable and unstable regions for operating conditions of the VR. This situation occurs because an internal model for the VR is lacking and product variations may cause parameters inside the VR to vary. Therefore, analyzing VR stability without prior knowledge of the VR internal model is challenging [9],[10]. Additionally, variation of load currents may also cause VR instability and inefficiency [9],[21]. Hence, an efficient and accurate failure region estimation method is necessary under the condition that the actual model is known.

### A. VR Mechanism

The two different types of VRs are linear (LVR) and switching VRs. LVRs are low cost and can regulate a small drop-out voltage with less noise compared with switching VRs [5],[6],[11]. Hence, LVR can minimize the amount of power loss in the internal VR and is highly efficient. VRs aim to regulate the input voltage supply and produce low-noise, constant, and stable output DC voltage [4],[5], thereby indicating the absence of multiple oscillations or ripples. Moreover, VRs can limit over- and undershoot values during sudden changes in the load current.

As shown in Fig. 1, a typical VR circuitry contains an output capacitor connected at the output terminal that acts as an energy storage element. Moreover, the output capacitor compensates for the disturbance during load transient [7],[8]. However, impurity element inside the capacitor called equivalent series resistance (ESR) is a main factor that contributes to the stability of the VR. Although a pure capacitor should ideally contain only the capacitance value without ohmic resistance, the case is different in the real world.

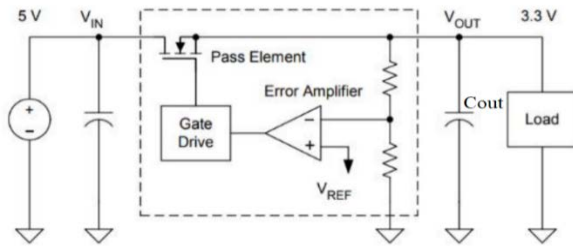


Fig. 1. Basic LVR Circuit.

### B. ESR Tunnel Graph

The optimum value of ESR is crucial in determining the stability of the VR. An excessively high or low value of ESR may cause a significant output voltage to undershoot, produce unwanted oscillations, and cause instability. The ESR compensates for the disturbance by adding zero to its transfer function to cancel out the non-dominant pole and thus achieve a dominant-pole compensation.

Manufacturers provide a datasheet for each fabricated VR to depict the stable range of ESR values in the VR circuit through a unique chart called the ESR tunnel graph. Fig. 2 shows an example of an ESR tunnel graph using the TPS76301, a commercial VR from Texas Instrument. The plot presents a range of ESR values against a range of load currents. A specific ESR and output current range is chosen for plotting the ESR tunnel graph. The figure shows that the value of ESR from  $0.3 \Omega$  to  $10 \Omega$  indicates a stable region while other values denote non-stable regions. The critical value of ESR is located at the failure region boundary.

### C. VR Stability Analysis

LVR stability can be analyzed using two types of responses: (a) load transient response in the time domain or (b) frequency response in the frequency domain. Stability analysis based on the load transient test is usually conducted because of its simplicity and the method can be performed under closed-loop condition despite its low accuracy [6]. Although the frequency response of the LVR can be ideally obtained when the system is under open-loop condition, this scenario is difficult to achieve in the actual case. The LVR system is typically packaged under closed-loop condition; therefore, yielding its transient response is simple [17]. Furthermore, the frequency response can yield a more accurate stability measurement than the transient response because it indicates the phase margin of the system [13],[18],[20]. However, determining the frequency response is challenging because it can only be obtained while the system is under open-loop condition and this scenario breaks the loop in the actual LVR. Thus, a method called noninvasive stability measurement (NSM) is proposed to obtain the frequency response of the VR system under closed-loop condition.

Studies on VR stability based on the NSM method are limited. Recent studies typically analyze the electronic system through transient response [5], [6], [16]. However, investigations based on the frequency response are few. Existing studies mainly focus on fault diagnosis [3], [12], [19], scalability, and dynamic performance [12] but those on achieving short-time stability analysis of VR are limited.

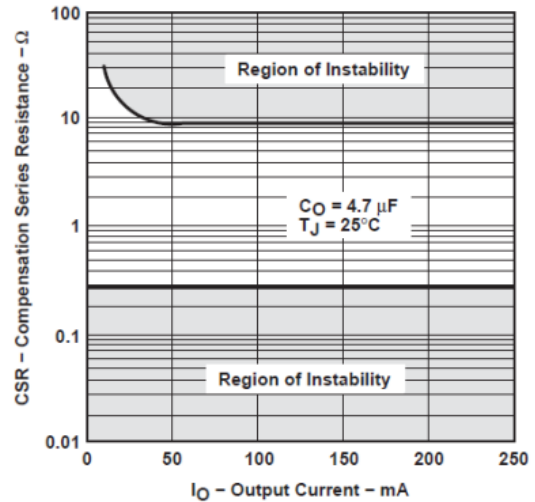


Fig. 2. Example of the ESR Tunnel Graph (VR Model TPS76301 from Texas Instruments).

NSM can be utilized to improve the existing stability characterization method in the VR failure region estimation process and determine the stability condition of a particular operating point. In addition, a virtual sensing approach that enhances the black-box modeling method can be used to illustrate the model of the internal VR circuitry and estimate the model transfer function coefficient used to determine critical ESR values located in the failure region boundary. Therefore, a model-based virtual sensing approach (MBA) that mainly focuses on the black-box modeling through system identification (SI) and training the neural network (NN) on the basis of the estimated transfer function coefficient is introduced in this study, as explained in Section II. MBA is used to estimate the internal model of the VR and reduce the number of data points required to estimate the critical value of ESR for generating the region of failure of the VR stability through the ESR tunnel graph. Furthermore, outcomes from this MBA approach are described and discussed in Section III.

## II. METHODS

Four phases of this study is presented in Fig. 3. The first phase is the manual characterization, which analyzes the load transient test of the VR. The outcome of this phase is also used as the benchmark for the proposed method in this work. The second phase implements the NSM method to obtain the phase margin of the VR circuit in each operating point in the ESR tunnel graph. The third phase applies the MBA by first estimating the VR system model using the system identification method and then training the neural network structure. The final phase validates the method performance using various performance metrics.

### A. VR Manual Characterization as Benchmark

The commercial LVR used in this study is the LT1963A from Analog Devices because of the comprehensive information provided in its datasheet [14] and its availability in the LTSpice software for simulation purposes. The LVR circuitry developed for the manual ESR characterization with a step signal is illustrated in Fig. 4. This step signal is used to

disturb the load current in the load transient test. The 10  $\mu\text{F}$  capacitor used in this work is based on the datasheet provided by manufacturers. A resistor is connected in series with the output capacitor and labeled ESR given that ESR is absent in the purely capacitive capacitor used in the simulation. As mentioned in the early section, VR characterization is performed manually in manufacturing practice. Hence, the ESR of the output capacitor manually varies and the undershoot, overshoot, and oscillations during the load transient test are observed for stability analysis.

The datasheet also indicated that the range of the input voltage should be between 2.5 and 20 V when obtaining the output voltage range of 1.21–20 V [14]. Therefore, two resistors (R1 and R2) must be chosen appropriately to obtain an output voltage of 5 V. Values of R1 and R2 can be calculated as follows:

$$V_{out} = V_{adj} \left( 1 + \frac{R_2}{R_1} \right) + (I_{adj})(R_2), \quad (1)$$

where  $V_{adj}$  is 1.21 V and  $I_{adj}$  is 3  $\mu\text{A}$ . Therefore, values obtained for R1 and R2 are 12 and 3.9 k, respectively.

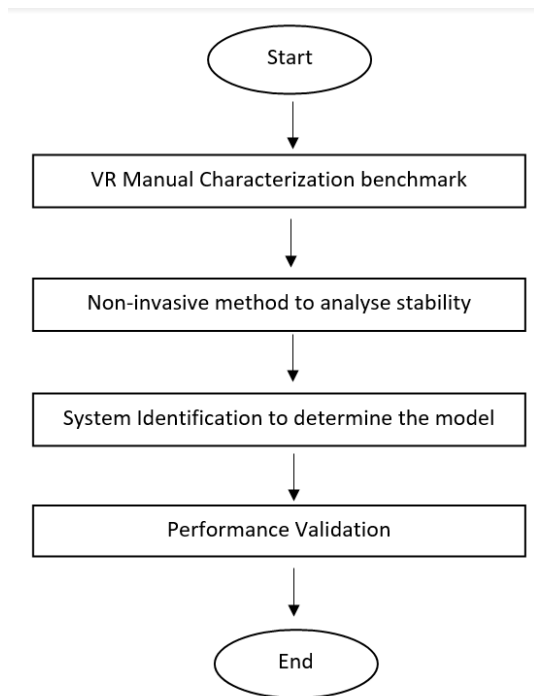


Fig. 3. Flowchart of the Proposed Method.

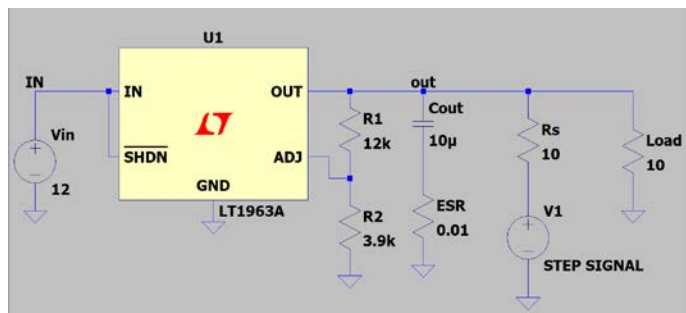


Fig. 4. LT1963A VR Circuit in LTSpice for Load Transient Test.

The ESR value is manually changed from 0.01  $\Omega$  to 0.3  $\Omega$ , with an increment of 0.01  $\Omega$ . Meanwhile, the load current is in the range of 0.01–0.05 A, with an increment of 0.01 A. Combining each ESR value and each load current produces one operating point. The load transient test is then conducted. The circuit is energized to obtain the transient response after the input voltage is initialized and the ESR and load current values are configured and set to a specific value. The start time is recorded immediately after the process begins until every operating point in the ESR tunnel graph is tested.

The stability of each operating point is determined manually on the basis of the output voltage observed in the load transient test response during the manual characterization. As stated in the LT1963A datasheet, the ESR value must be between 20 m $\Omega$  and 3  $\Omega$  for an output voltage of 1.2 V with a 10  $\mu\text{F}$  output capacitor to ensure VR stability [14]. The output voltage oscillation must be examined for each operating data point in this case. Otherwise, the VR system is considered unstable with excessive ringing, that is, more than three oscillations exist. This stability condition check is also performed manually and requires high expertise. Manual characterization is conducted on all data points. Finally, an ESR tunnel graph is illustrated to depict stable and unstable ranges of ESR for a specific load current.

### B. Noninvasive Stability Measurement

The proposed stability measurement method is based on the NSM method, which analyzes the VR stability under closed-loop condition to obtain the phase margin of the VR system. Fig. 5 shows the LVR circuitry setup to obtain the phase margin from the frequency response of the LVR system using a small-injection AC signal with an injection transformer at the output terminal of the LVR.

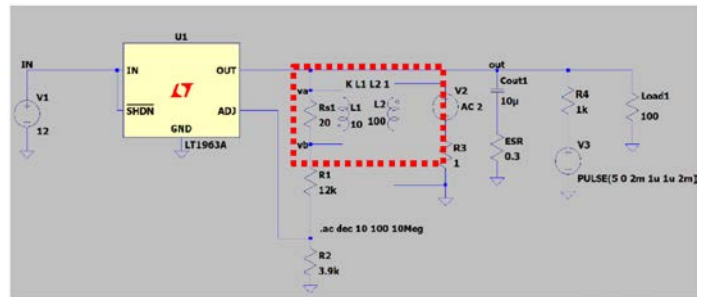


Fig. 5. LVR Circuitry for Noninvasive Stability Measurement.

The NSM method is proposed to obtain the phase margin through frequency response without breaking the loop condition of the system. Thus, the result obtained from this approach is accurate and efficient because breaking the control loop of the VR system is unnecessary. A small-injection resistor  $R_{inj}$  with a value of 20  $\Omega$ , which is relatively small compared with that of R1 and R2, is connected in series at the upper terminal of R1 to perform the NSM method and ensure that two different injection points ( $v_a$  and  $v_b$ ) can be established. A ground (GND) reference for these points is absent; therefore, an injection transformer is connected parallel to  $R_{inj}$  on the primary side  $L1$ . Meanwhile, the secondary side  $L2$  is connected to a sine wave signal generator V2. Both points  $v_a$  and  $v_b$  are then connected to an oscilloscope to ensure

that both sine wave signals entering the system at point  $v_b$  and exiting the system at point  $v_a$  can be observed. Amplitude gains of both sine wave signals are expected to differ; thus, frequency tuning is required until both sine waves display the same gain, which is equal to 1 or also known as unity gain. The frequency when both sine wave channels demonstrate the same gain is known as crossover frequency at 0 db or unity gain frequency. Another parameter that must be considered is the phase shift between the two signal waves at points  $v_a$  and  $v_b$ . The phase shift value between the two signal waves represents the phase margin of the system. Therefore, the ESR tunnel graph can be produced by observing the system's frequency response for each operating data point tested using the NSM method and an accurate stability condition is expected.

### C. VR System Modeling Through SI

The next step is to apply the black-box modeling approach through SI to estimate the VR circuit model. The SI method is used to estimate the internal model of the VR circuit given that input and output data are available [15]. The circuit used for SI data acquisition is similar to the one displayed in Fig. 4. However, the voltage source V1 in Fig. 4 generates a pseudorandom binary signal (PRBS) instead of a step signal in SI. Steps taken in the SI approach are the preprocessing of data, estimation and validation of data, model structure determination, and choosing the desired coefficient of the model. Hence, the model of the VR system can be evaluated with the optimal fitness model.

Input, output, and sampling time must be determined prior to data preprocessing. In this case, input data are the small-signal output voltage  $V_{out}$  and output data are the small-signal output current  $I_{out}$ . These data are obtained from the circuit simulation using LTSpice by exporting all data into the MATLAB software. Further processing is then conducted in MATLAB. The removal of the mean value of raw data after importing raw data is also known as detrend. Half of detrended data is used for estimation data while the other half is utilized for validation data.

The SI model structure selection must be determined for estimating the VR model. Several types of model structures, such as autoregressive exogenous input (ARX), output-error (OE), autoregressive moving average exogenous input (ARMAX), and Box-Jenkins (BJ) model structures, can be used to estimate the model of a dynamic system [7], [8]. This work utilized the OE model structure due to its simpler model transfer function parameters compared with those of other model structures. Fig. 6 shows the output-error model structure.

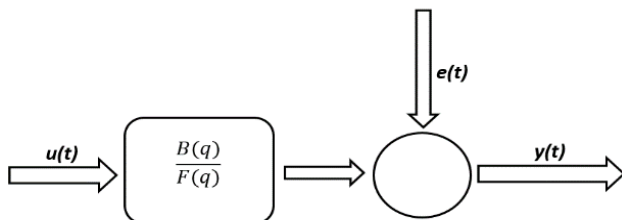


Fig. 6. OE Model Structure.

The OE model structure can be expressed as follows:

$$y(t) = \frac{B(q)}{F(q)}u(t - n_k) + e(t) \quad (2)$$

where  $y(t)$  is the model output,  $u(t)$  is the model input,  $n_k$  is the number of delays,  $e_k$  is the white noise error, and  $k$  is the number of samples. In addition, the polynomial  $B(q)$  represents the numerator in relation to the input  $u(t)$  and  $F(q)$  represents the denominator in relation to the output  $y(t)$ . Polynomials  $B(q)$  and  $F(q)$  can be expressed with the backward shift operator term  $q^{-1}$  as follows:

$$B(q) = \sum_{k=1}^{\infty} b_k q^{-k} = b_1 + b_2 q^{-1} + \dots + b_{n_b} q^{-n_b+1}, \quad (3)$$

$$F(q) = \sum_{k=0}^{n_f} f_k q^{-k} = 1 + f_1 q^{-1} + \dots + f_{n_f} q^{-n_f}, \quad (4)$$

where  $n_b$  is the order of polynomial  $B(q)$  and  $n_f$  is the order of polynomial  $F(q)$ . The following process is used for model estimation using the linear regression for an iterative method with unknown parameters  $\theta$ :

$$y(k, \theta) = \phi(k^T)\theta = \frac{B(q)}{F(q)}u(t) = \xi(k, \theta), \quad (5)$$

where  $\phi(k)$  is expressed as

$$\phi(k) = [u(k-1), u(k-2), \dots, u(k-n_b), -\xi(k-1, \theta), -\xi(k-2, \theta), \dots, -\xi(k-n_f, \theta)], \quad (6)$$

where  $\theta$  is expressed as

$$\theta = [b_1, b_2, \dots, b_{n_b}, f_1, f_2, \dots, f_{n_f}]^T \quad (7)$$

Therefore, the percentage error of actual output data and the estimated output model can be reduced by obtaining the model transfer function coefficient or parameter vector  $\theta$ . We then apply validation data to the estimated transfer function. Hence, the model fitness can be obtained and the transfer function with the maximum percentage of the fitness model is selected. Validation of the selected SI model transfer function is continued with a step signal that changes from 0 V to 5 V after a slight delay. The transient response from SI is recorded and then compared with the one in the LVR circuitry simulation during the load transient test to validate the SI-estimated model.

### D. Neural Network Training

The following process shows the training of the NN structure to reduce the number of operating points by testing the few sets of operating data points. Therefore, VR characterization time can be significantly reduced with the decrease of testing of operating data points. Fig. 7 shows an example of an NN structure consisting of input, hidden, and output layers with a number of neurons.

Input data are fed into the NN structure via channels, which are typically assigned with numerical values and known as the weight, to the hidden layer in this stage. Input layers are then multiplied to their own corresponding weights, and the hidden layer performs its mathematical computation. The output layer predicts the output, which is the estimated model transfer function coefficients previously obtained from the SI. Finally, the ESR and load currents are fed into the input layer while

transfer function coefficients of the SI model are fed into the output layer. These input selections are chosen due to their correlation with the coefficient of the output transfer function for each operating data point in the ESR tunnel graph.

The trained NN structure was then used to estimate the model transfer function for the remaining untested operating data. The step response was obtained through MATLAB simulation for each operating data point after estimating all transfer function coefficients using the trained NN. Step responses from both manual characterization and MBA (SI-NN) are then compared and validated for their similarity. Finally, an ESR tunnel graph from the MBA-based characterization is produced and then compared with the ESR tunnel graph from the manual characterization in terms of critical ESR values.

### E. Performance Validation

The last stage evaluates the obtained ESR critical values from both manual and MBVS characterization processes and determines the efficiency of the MBVA characterization method compared with the manual process. Mean squared error (MSE), root mean squared error (RMSE), mean absolute error (MAE), correlation coefficient ( $R^2$ ), and efficiency calculation can be expressed as follows:

$$MSE = \frac{1}{N} \sum_{i=1}^n [y(i) - y_p(i)]^2, \quad (8)$$

$$RMSE = \sqrt{\frac{1}{N} \sum_{i=1}^n [y(i) - y_p(i)]^2}, \quad (9)$$

$$MAE = \frac{1}{N} \sum_{i=1}^n |y(i) - y_p(i)|, \quad (10)$$

$$R^2 = \frac{\sum_{i=1}^n (y(i) - \bar{y}(i))(y_p(i) - \bar{y}_p(i))}{\sqrt{\sum_{i=1}^n (y(i) - \bar{y}(i))^2 \sum_{i=1}^n (y_p(i) - \bar{y}_p(i))^2}}, \quad (11)$$

$$Efficiency = \left[ 1 - \frac{t_{SI-NN}}{t_{manual}} \right] \times 100\%, \quad (12)$$

where the term  $y$  is the actual critical ESR value,  $y_p$  is the critical ESR value obtained from the proposed method,  $n$  is the number of observations, and  $i$  is the number of load current instants. The output of the proposed method is the SI-NN characterization and validated if MSE, RMSE, and MAE values are close to zero. The efficiency value determines how the time is taken for the proposed method to be conducted compared to the manual characterization method.

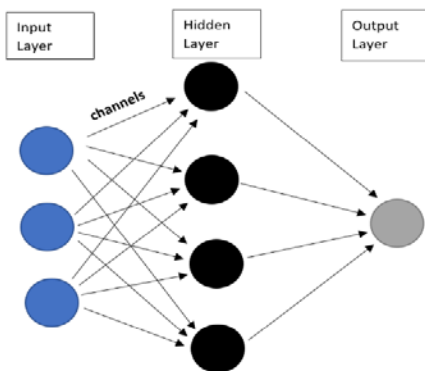


Fig. 7. Neural Network Structure.

## III. RESULTS AND DISCUSSION

### A. Manual VR Characterization Results

This stage phase aims to produce a benchmark for the ESR tunnel graph that depicts stable and unstable regions of operating data points. As mentioned earlier, the ESR value must be higher than 20 mΩ for an output voltage of 1.2 V to ensure VR stability. The load transient of the LVR circuit is simulated and then the transient response is observed to analyze its corresponding number of oscillations at this operating condition. Fig. 8 shows the transient response obtained from the load transient for an LVR circuit with an output current of 500 mA, ESR value of 20 mΩ, and output voltage of 1.2 V. As shown in Fig. 8, the number of oscillations obtained is three cycles with an undershoot of 31.34 mV.

A voltage drop of 31.34 mV is observed from the first wave of the load transient. Stability analysis is carried out using the noninvasive method under closed-loop conditions after the load transient is obtained from the circuit simulation for each operating data point to provide increasingly accurate and efficient stability measurement through the system's frequency response. Fig. 9 depicts the Bode plot to obtain the phase margin of the system through the frequency domain. Component parameters of the circuit for this noninvasive method are the same as those used to obtain the load transient test circuit.

The phase margin obtained from the noninvasive method was 17.64° at a crossover frequency of 206.28 kHz. This phase margin value indicates the border region of the system stability. Hence, an ESR tunnel graph depicted in Fig. 10 is the product of all operating data points tested using the noninvasive method.

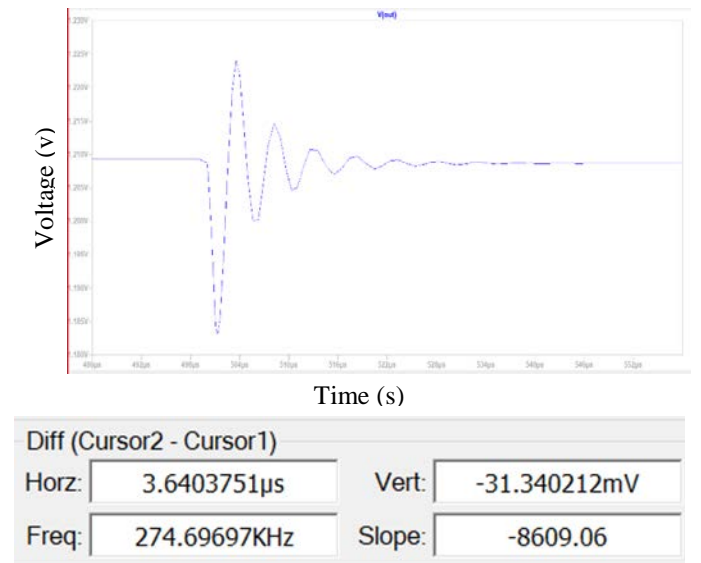


Fig. 8. Transient Response for an Output Current of 500 mA with an ESR of 20 mΩ.

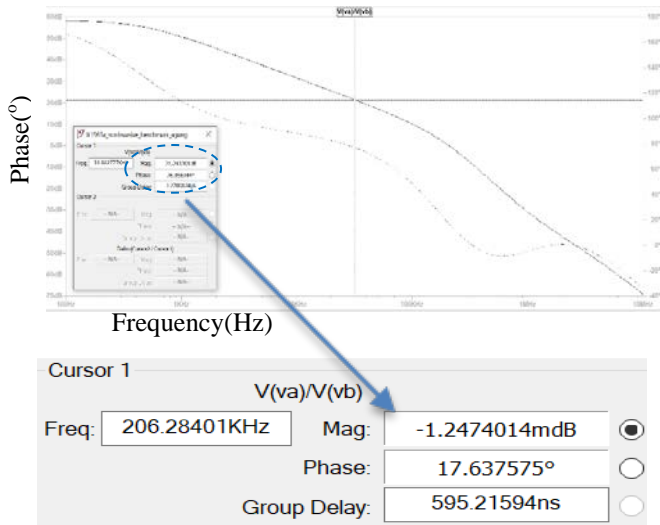


Fig. 9. Phase Margin Results using the Noninvasive Method.

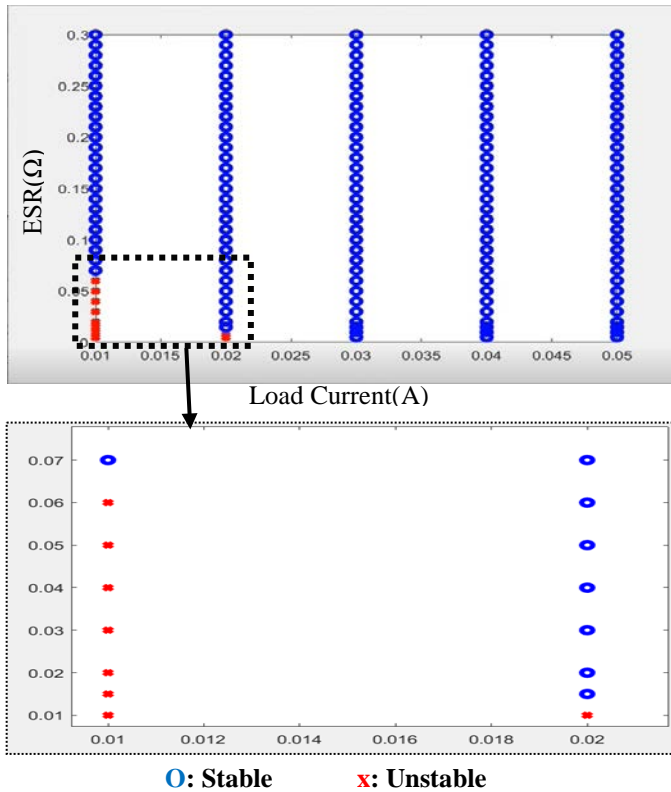


Fig. 10. ESR Tunnel Graph through Manual Characterization.

**B. SI-NN Characterization Results**

The SI-NN characterization method is approached after the manual benchmark has been obtained. First, the SI method uses the black-box modeling concept to determine the transfer function coefficient that represents the system model. Second, the model selection with the maximum percentage of model fitness is selected to represent the system model. Fig. 11 shows the output model fitness by tuning parameters of poles and zeroes of the OE models. The percentage fitness of different model parameters of OE is presented in Table I.

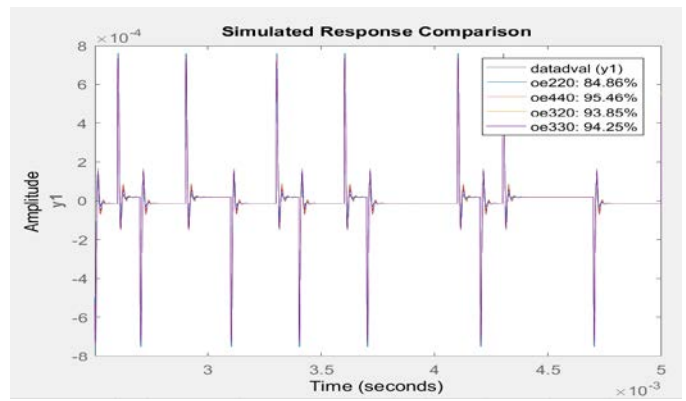


Fig. 11. Output Models with Fitness Percentage.

TABLE I. FITNESS PERCENTAGE OF DIFFERENT MODELS

Model	Fitness Percentage (%)
OE220	84.86
OE320	93.85
OE330	94.25
OE440	95.46

The model fitness percentage with the minimum number of parameters is chosen due to its simplicity. Thus, the OE320 model is selected. The output yields a transfer function coefficient for  $B(q)$  and  $F(q)$  parameters on the basis of this model (Fig. 12). Finally, the transfer function coefficient is tabulated and used for NN training and the dataset reduction phase.

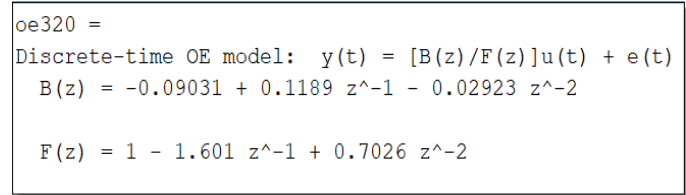


Fig. 12. Transfer Function Coefficient for OE320.

All individual coefficients are applied to the output of the NN structure after the transfer function coefficient obtained from all operating data points is characterized and tabulated through SI to validate the output model. All individual transfer function coefficients are combined and fed into the output layer of the NN structure. Therefore, the value of the NN output layer is 5. Finally, as mentioned earlier, the ESR and output current are fed to the input layer of the NN. Thus, the input layer is 2, and the hidden layer varies from 10 to 50 with an increment of 10. Fig. 13 shows the network architecture of an NN structure trained for the selected estimated model.

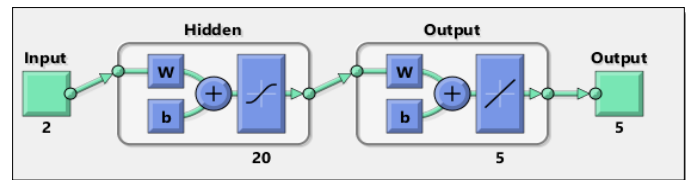


Fig. 13. NN Structure.

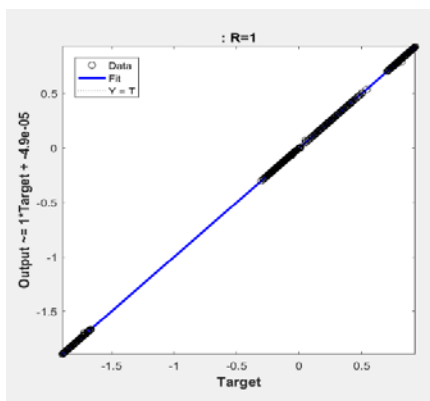


Fig. 14. Regression Plot.

The dataset used for training into the NN varies by reducing the percentage of the total dataset from the SI beginning with 93.7%, 87.5%, 81.25%, 75%, and 68.75%. For each of the reduced percentage dataset reductions, a different number of hidden layers, as mentioned earlier, is assigned to train the neural network structure starting. Bayesian regularization (BR) is then used as the training algorithm. Fig. 14 illustrates the regression plot of the output data obtained. The value of  $R^2$  indicates the correlation between measured and target outputs. A value approaching 1 indicates a close and precise relationship.

### C. ESR Tunnel Graph using SI-NN

The ESR tunnel graph benchmark from manual characterization is then compared with the ESR tunnel graph obtained using the SI-NN characterization, with the phase margin as the targeted output. Fig. 15 shows the ESR tunnel graph obtained from the SI-NN approach.

### D. Performance Metrics

Performance metric parameters in Tables II and III were observed for a different number of dataset reductions and a fixed hidden layer size of 20 and 10, respectively, to validate the results of the SI-NN characterization method further.

The calculated metrics showed that at 20 number of trained data, for hidden layer size of 20, yields the most negligible MSE value of  $5 \times 10^{-6}$  that showed a high critical ESR value prediction.

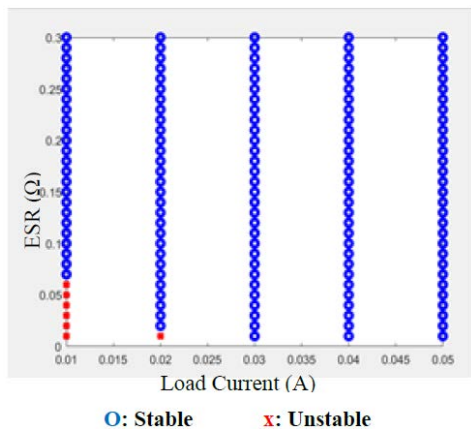


Fig. 15. ESR Tunnel Graph using the SI-NN Approach.

TABLE II. PERFORMANCE METRICS FOR DIFFERENT NUMBERS OF REDUCED TRAINED DATA AT A HIDDEN LAYER SIZE OF 20

No. of trained data	Performance Metrics			
	MSE	RMSE	MAE	$R^2$
10	$5 \times 10^{-5}$	$7.07 \times 10^{-3}$	$2 \times 10^{-3}$	0.987
20	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.999
30	$4.5 \times 10^{-5}$	$6.71 \times 10^{-3}$	$3 \times 10^{-3}$	0.999
40	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.999
50	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.999

TABLE III. PERFORMANCE METRICS FOR DIFFERENT NUMBERS OF REDUCED TRAINED DATA AT A HIDDEN LAYER SIZE OF 10

No. of trained data	Performance Metrics			
	MSE	RMSE	MAE	$R^2$
10	$6.85 \times 10^{-4}$	$2.62 \times 10^{-2}$	$1.5 \times 10^{-2}$	0.99
20	$2.5 \times 10^{-4}$	$5 \times 10^{-3}$	$3 \times 10^{-3}$	0.91
30	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.99
40	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.99
50	$5 \times 10^{-6}$	$2.24 \times 10^{-3}$	$1 \times 10^{-3}$	0.99

## IV. CONCLUSION

The proposed method can generally reduce the amount of time taken to characterize the failure region of the voltage regulator, and estimate critical ESR values that accurately distinguish stable and unstable regions of the voltage regulator system. The proposed method can estimate the internal model of VR through the SI method. Furthermore, the VR output voltage stability can be determined via a noninvasive stability measurement approach without breaking the internal control loop inside the VR circuit.

## ACKNOWLEDGMENT

The authors acknowledge the financial support received from the Ministry of Higher Education Malaysia through research grant no. FRGS/1/2019/TK04/UKM/03/1.

## REFERENCES

- [1] M. H. Jahanbakhshi & M. Etezadinejad. 2019. Modeling and current balancing of interleaved buck converter using single current sensor. *27<sup>th</sup> Iranian Conference on Electrical Engineering (ICEE2019)*, pp. 662-667.
- [2] O. Garcia, P. Zumel, A. de Castro, P. Alou & J. Cobos. A. 2008. Current self-balance mechanism in multiphase buck converter. *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 624-628.
- [3] I. Kovacs, M. Topa, M. Ene, A. Buzo & G. Pelz. 2020. A metamodel-based adaptive sampling approach for efficient failure region characterization of integrated circuits. *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, pp. 1-5.
- [4] M. H. M. Zaman, M. M. Mustafa, M. A. Hannan & A. Hussain. 2018. Neural network based prediction of stable equivalent series resistance in voltage regulator characterization. *Bulletin of Electrical Engineering and Informatics*, vol.7, no.1, pp. 134-142.
- [5] N. Sedaghati, H. Martinez-Garcia & J. Cosp-Vilella. 2016. On modeling of linear assisted DC-DC voltage regulators. *2016 Conference on Design of Circuits and Integrated Systems (DCIS)*, pp. 1-4.
- [6] X. Ming, H. Liang, Z. W. Zhang, Y. L. Xin, Y. Qin & Z. Wang. A High Efficiency and Fast-Transient Low-Dropout Regulator With Adaptive Pole Tracking Frequency Compensation Technique. *IEEE Transactions on Power Electronics*, vol.35, no.11, pp. 12401-12415, 2020.

- [7] M. H. M. Zaman, M. M. Mustafa & A. Hussain. 2018. Estimation of voltage regulator stable region using radial basis function neural network. *Journal of Telecommunication, Electronic and Computer Engineering*, vol.10, no.2-8, pp.63-66.
- [8] M. H. M. Zaman, M. M. Mustafa & A. Hussain. 2017. Critical equivalent series resistance estimation for voltage regulator stability using hybrid system identification and neural network. *International Journal on Advanced Science, Engineering and Information Technology*, vol.7, no.4, pp.1381-1388.
- [9] C. Wang, C. Huang, T. Lee & U. F. Chio. 2006. A linear LDO regulator with modified NMCF frequency compensation independent of off-chip capacitor and ESR. *APCCAS 2006-2006 IEEE Asia Pacific Conference on Circuits and Systems*. pp. 880-883.
- [10] M. Day. 2002. Understanding low drop out (LDO) regulators. *Texas Instruments, Dallas*. pp. 1-6.
- [11] N. Tang, Y. Tang, Z. Zhou, B. Nguyen, W. Hong, P. Zhang, J. H. Kim & D. Heo. 2018. Analog-assisted digital capacitorless low-dropout regulator supporting wide load range. *IEEE Transactions on Industrial Electronics* 2019, vol. 66, no. 3, pp. 1799-1808.
- [12] K. Laadjal & M. Sahraoui. 2020. On-Line fault diagnosis of DC-Link electrolytic capacitors in boost converters using the STFT technique. *IEEE Transactions on Power Electronics* 2021, vol. 36, no. 6, pp. 6303-6312.
- [13] M. Ho, J. Guo, K. H. Mak, W. L. Goh, S. Bu, Y. Zheng, X. Tang & K. N. Leung. 2016. A CMOS low-dropout regulator with dominant pole-substitution. *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6362-6371.
- [14] LT1963A series: 1.5A, low noise, fast transient response LDO regulators data sheet. California, United States of America.
- [15] T. Souvignet, T. Coulot, Y. David, S. Trochut, T. Di Gilio & B. Allard. 2013. Black box small-signal model of PMOS LDO voltage regulator. *IECON 2013-39<sup>th</sup> Annual Conference of the IEEE Industrial Electronics Society*, pp. 495-500.
- [16] Y. Li, H. Fan, Q. Feng, Q. Hu, L. Hu, H. Chen & H. Heidari. 2020. A fast transient response and high PSR low drop-out voltage regulator. *27<sup>th</sup> IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 1-4.
- [17] B. Dennis & B. S. Kariyappa. 2018. Fault isolation in analog circuits using multi-support vector neural network. *3rd International Conference on Communication and Electronics Systems (ICCES)*, pp. 655-660.
- [18] B. Dennis & B. S. Kariyappa. 2018. Support vector neural network and principal component analysis for fault diagnosis of analog circuits. *2nd International Conference on Trends in Electronics and Informatics (ICOEI)*, pp. 1152-1157.
- [19] C. Yang, X. Zhang, A. He & L. Qiu. 2017. Fault diagnosis of analog circuit based on complex model. *32nd Youth Academic Annual Conference of Chinese Association of Automation (YAC)*, pp. 949-952.
- [20] Y. K. Cho & B. H. Park. 2015. Loop stability compensation technique for continuous-time common-mode feedback circuits. *International SoC Design Conference (ISOCC)*, pp. 241-242.
- [21] M. Dobler, M. Harrant, M. Rafaila, G. Pelz, W. Rosenstiel & M. Bogdan. 2015. Bordersearch: An adaptive identification of failure regions. *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2015, pp. 1036-1041.