A Novel Technique for Glitch and Leakage Power Reduction in CMOS VLSI Circuits

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***Abstract*—Leakage power has become a serious concern in nanometer CMOS technologies. Dynamic and leakage power both are the main contributors to the total power consumption. In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. In this paper, a technique has been proposed which will reduce simultaneously both glitch and leakage power. The results are simulated in Microwind3.1 in 90nm and 250 nm technology at room temperature.**

Keywords-*Dynamic power; Leakage power; Multi-threshold; Variable body biasing; Glitch.*

I. INTRODUCTION

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology, but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current.

Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power.

According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, in this paper a novel approaches for reducing both leakage and dynamic power with minimum possible area and delay tradeoff are proposed.

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic (switching) power dissipation. However, the subthreshold leakage current increases exponentially thereby increasing static power dissipation [1].

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18µ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.09µ and 0.065µ, static power has become a great challenge for current and future technologies.

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. Power consumption has two components: Dynamic Power and Leakage power [2]. Dynamic and leakage power both are the main contributors to the total power consumption. Dynamic power includes both switching power and short circuit power. Spurious transitions (also called glitches) in combinational CMOS logic are a well-known source of unnecessary power dissipation. Reducing glitch power is a highly desirable target [3]. The dynamic power cannot be eliminated completely, because it is caused by the computing activity. It can, however, be reduced by circuit design techniques.

Static power refers to the power dissipation which results from the current leakage produced by CMOS transistor parasitic. Traditionally static power has been overshadowed by dynamic power consumption, but as transistor sizes continue to shrink, static power may overtake dynamic power consumption To alleviate the rising significance of static power in digital systems, static power reduction technique shave been developed like transistor stacking, dual threshold voltage , MTCMOS etc. Some of these techniques are state saving and some are state destructive techniques. For example: Sleep transistor is a state destructive technique. Despite the rising significance of static power in CMOS circuits, the dynamic power is still the major contributor to power consumption. Dynamic power is mostly consumed by glitches which are the unwanted transitions and need to be eliminated.

Glitch and leakage power both are the main contributors to the power consumption and needs to be reduced.

II. Power Dissipation Factors

In CMOS, power consumption consists of leakage power and dynamic power Dynamic power includes both switching power and short circuit power. Switching power is consumed when the transistors are in active mode and short circuit power is consume when a pull-up and pull-down network are on turning on and off. For 0.18u and above leakage power is small compared to dynamic power but 0.13u and below leakage power is dominant. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation [4].

Static power dissipation is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The subthreshold leakage current increases exponentially, thereby increasing static power dissipation.

The leakage current of a transistor is mainly the result of reverse biased PN junction leakage and Sub threshold leakage. Compared to the subthreshold leakage, the reverse bias PN junction leakage can be ignored. The Subthreshold conduction or the subthreshold leakage or the subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage [5].

It is given by:

$$I_{sub} = I_{so} \exp\left(\frac{V_{gs} - V_{th}}{V_T}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (1)$$

$$I_{s0} = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} \quad (2)$$

where μ_0 is the zero bias electron mobility, n is the subthreshold slope coefficient, V_{gs} and V_{ds} are the gate to source voltage and drain-to-source voltage, respectively, V_T is the thermal voltage, V_{th} is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and W_{eff} and L_{eff} are the effective channel width and length, respectively. Due to the exponential relation between V_{th} and I_{sub}, an increase in V_{th} sharply reduces the subthreshold current.

A. Leakage Current Reduction

Reduction in threshold voltage results in the increase in sub-threshold leakage current. One of challenge with technology scaling is the rapid increase in subthreshold leakage power due to V_t reduction. In such a system it becomes crucial to identify techniques to reduce this leakage power component. The development of digital integrated circuits is challenged by higher power consumption [6].

Leakage current is a primary concern for low-power, high-performance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling, which is essential to maintain high performance in active mode, since supply voltages are scaled. Numerous design techniques have been proposed to reduce standby leakage in digital circuits. Leakage power has become a serious concern in nanometer CMOS technologies, and power-gating has shown to offer a viable solution to the problem with a small penalty in performance [7].

Devices which are operated on battery are either idle (Standby) or Active mode. Leakage power can be divided in to two categories based on these two modes [8]:

1) Leakage Control in Standby Mode: Techniques like Power gating and super cutoff CMOS are used for leakage reduction in standby mode. In these techniques, circuit is cutoff from the supply rails, when it is in idle state.

2) Leakage Control in Active Mode: Techniques like forced stacking and sleepy stack can be used during the run time or active mode for leakage current reduction.

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology. To reduce leakage power, many techniques have been proposed, including dual-Vth, multi-Vth, optimal standby input vector selection, transistor stacking, and body bias.

Multiple thresholds can be used to deal with the leakage problem in low-voltage high-performance CMOS circuits. The dual-V_{th} assignment is an efficient technique for decreasing leakage power. In this method, each cell in the standard cell library has two versions, low Vthand high Vth. Gates with low Vthare fast, but have high subthreshold leakage, whereas gates with high Vthare slower but have much reduced subthreshold leakage. The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry. The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity [9]. Already existing methods like stack, sleepy stack, and sleep transistor are shown in Fig. 1-3.

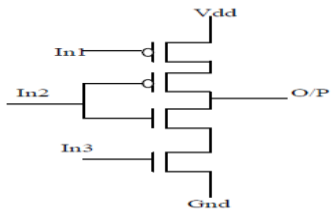


Figure 1. Sleep Transistor.

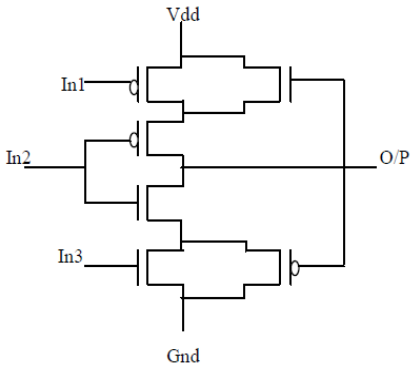


Figure 2.Sleepy Keeper.

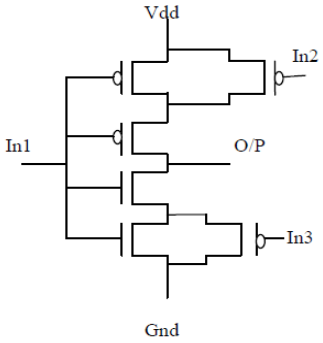


Figure 3.Sleepy Stack.

Circuit optimization provides low power and high performance. Circuit optimization can be obtained through simultaneous gate sizing and threshold voltage (Vt) assignment [10,11]. The sleep transistors areturned off when the logic circuits are not in use. By isolating the logic networks using sleeptransistors, the sleep transistor technique dramatically reduces leakage power during sleepmode.Sleep transistor method provides good reduction in leakage power, but it is a state destructive technique. It is shown in Fig. 1.

State -destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. Both dynamic and leakage power reductions can be achieved through threshold voltage adjustment [12]. Sleepy keeper technique shown in Fig. 2 uses the traditional sleep transistors with two additional transistors to save state during sleep mode. Dual threshold voltages can also be applied in the sleepy keeper approach to reduce subthreshold leakage current [13].The sleepy stack approach combines the sleep and stack approaches. The stack approach uses a stack effect by breaking down an existing transistor into two half size transistors [14, 15, 16]. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Fig. 3 shows its structure.

B. CMOS Glitch Elimination

One of the major factors contributing to the power dissipation in CMOS digital circuits is the switching activity. Dynamic power comprises of two parts: Logic switching power and glitch power. Whenever a logic gate changes state, power is consumed. The state change can be due to the essential logic value changes as well as due to glitches. Every signal transition consumes a finite amount of energy. For the correct functioning of a logic circuit, every signal needs to transition at most one time in one clock cycle. But in reality, the gate outputs transition more than once and these unnecessary transitions are called glitches. These transitions consume energy and are quite unnecessary for the correct functioning of the circuit.

Because switching power consumed by the gate is directly proportional to the number of output transitions, glitches reportedly account for 20%– 70% dynamic power. Delay elements are components inserted into a digital circuit that do not alter the signal value, but deliver the same waveform at the output with some extra delay. Different delay elements can be used to insert delay at the inputs of gate. By inserting these delay elements glitches can be eliminated. A buffer is the simplest of the delay elements. Insertion of the buffer as the delay element is one of the way to remove glitches or unwanted transitions. Buffer as delay elements are simple and reliable, but their problem is increased dynamic power. NMOS, Transmission Gate, Cascaded Inverters are some of the other delay elements.

A combinational circuit is minimum transient energy design, i.e., there is no glitch at the output of any gate, if the difference of the signal arrival times at every gate's inputs remains smaller than the inertial delay of the gate. Hazard filtering, when used alone for glitch elimination, can increase the overall input to output delay. Path balancing does not increase the delay but requires insertion of delay elements. A combination of the two procedures can give an optimum design.

III. PROPOSED MODEL

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift, where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static and Dynamic Power. Static (Leakage) power: includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling.

Among these, subthreshold leakage is the most prominent one. Dynamic power: Includes charging and discharging (switching) power and short circuit power. In Dynamic power, power consumption due to switching activity is more prominent. It can be concluded from the above discussion so far that glitch and leakage power both are the main contributors to the power consumption.

The existing leakage reduction techniques like sleep transistor, sleepy keeper, stack etc. are having the drawbacks like: increased delay, area etc. and the buffer used as delay elements for elimination of glitches also has the drawbacks of large area overhead and increases the number of transitions in the output. Therefore, in this section new approach has been proposed keeping in mind all the drawbacks mentioned above, which will simultaneously reduce both glitch and leakage power.

A novel technique has been proposed in this section, which will reduce both glitch and leakage power in CMOS VLSI circuits. The new technique is Sleep Variable body biasing with transmission gate. The circuit diagram of unoptimized circuit 1 and optimized circuit 1 is shown in the Fig.4-5.

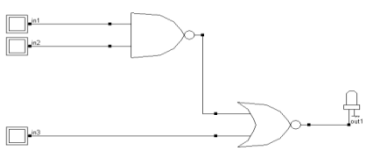


Figure 4.Unoptimized Circuit 1.

This proposed design includes variable body biasing technique along with sleep insertion technique. Sleep transistors are crucial part in any low leakage power design. The source of one of the sleep transistor is connected to the body of other PMOS sleep transistor for having body biasing effect. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. This technique uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor. Due to the minimum aspect ratio the sub-threshold current reduces.

Since the sources of the NMOS sleep transistor is connected to the body of PMOS transistor as shown in Fig. 5, the threshold voltage of the sleep transistors increases due to the body biasing effect during sleep mode. This increase of threshold voltage of the transistors reduces the leakage current. That's why the static power consumption also lowers.

The variable biasing will be useful in reducing leakage power. Sleep transistor method provides good reduction in leakage power in idle mode, but it is a state destructive technique.

Stacking approach is also utilized here to some extent to retain the state in active mode. Variable body biasing will be useful in increasing threshold voltage to reduce leakage current.

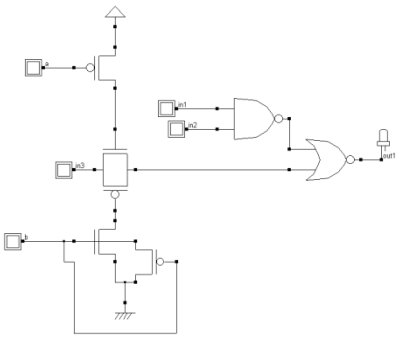


Figure 5.Optimized Circuit 1.

For the reduction of glitch power a transmission gate is also included. The transmission gate is used as a delay element for the elimination of the glitches. The transmission gate has a less area overhead as compared to other delay elements.

The technique has been used on non-critical paths to reduce glitches.

Consider another circuit diagramunoptimized circuit 2 shown in Fig. 6 [2]. The output of this circuit also has glitches, which is a waste of energy. Glitches are occurring because there is difference in the signal arrival times at the inputs of gate. The proposed technique is also applied in this circuit. This circuit is simulated in both 250nm and 90nm technology.

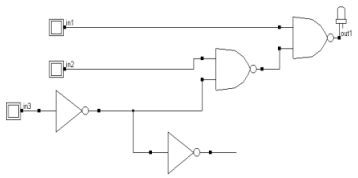


Figure 6.Unoptimized Circuit 2 [2].

The proposed technique is applied in the unoptimized circuit shown in Fig. 6. The optimized circuit is shown in Fig. 7.Transmission gate used here in the proposed technique is useful for eliminating glitches present in the output of unoptimized circuit.

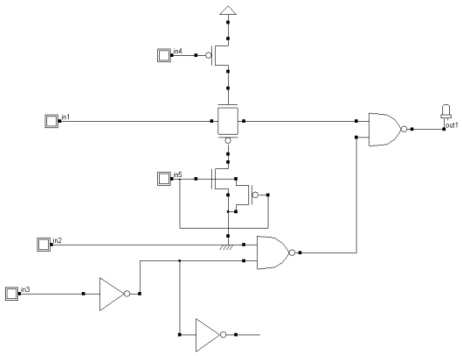


Figure 7.Optimized Circuit 2.

IV. Results And Conclusions

In this section, simulations of the proposed methods Comparisons between optimized and unoptimized circuit are shown in tabular form. Simulations are obtained in Microwind Tool. First step in obtaining the simulations is to compile the Verilog file in Microwind 3.1.

Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Microwind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Microwind. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature.

Simulations of circuits given in Fig. 4-7 are shown below in Fig.8-13.Simulations shown in these figures include the waveform of Voltage vs. Time and Voltage vs. Current. Simulations for unoptimized and optimized circuit 2 shown in Fig. 6-7 are given for both 250 and 90 nm technology.

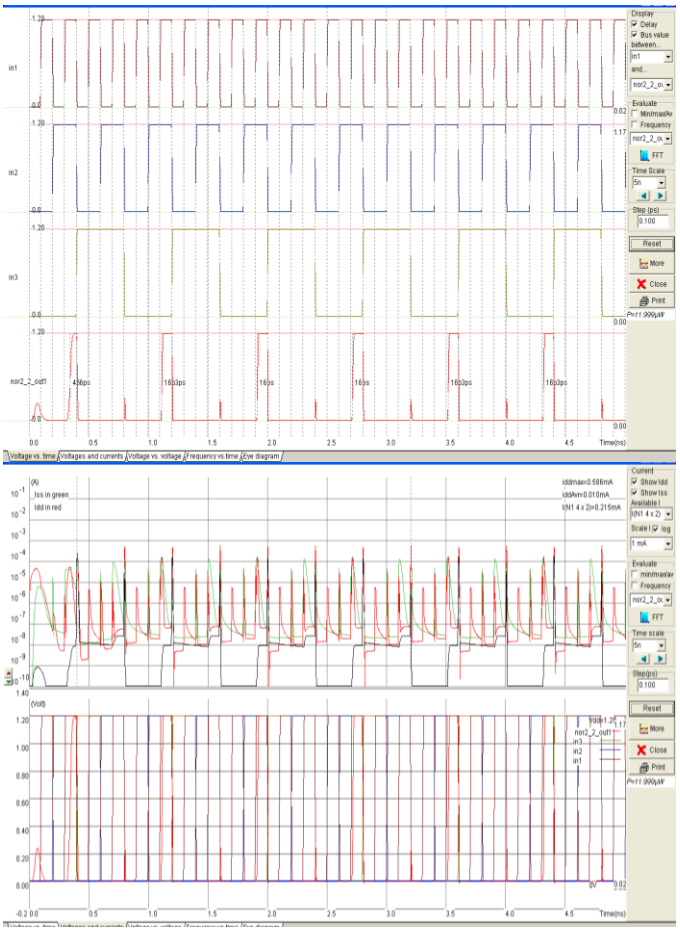


Figure 8.Simulations of Unoptimized Circuit 1(90 nm).

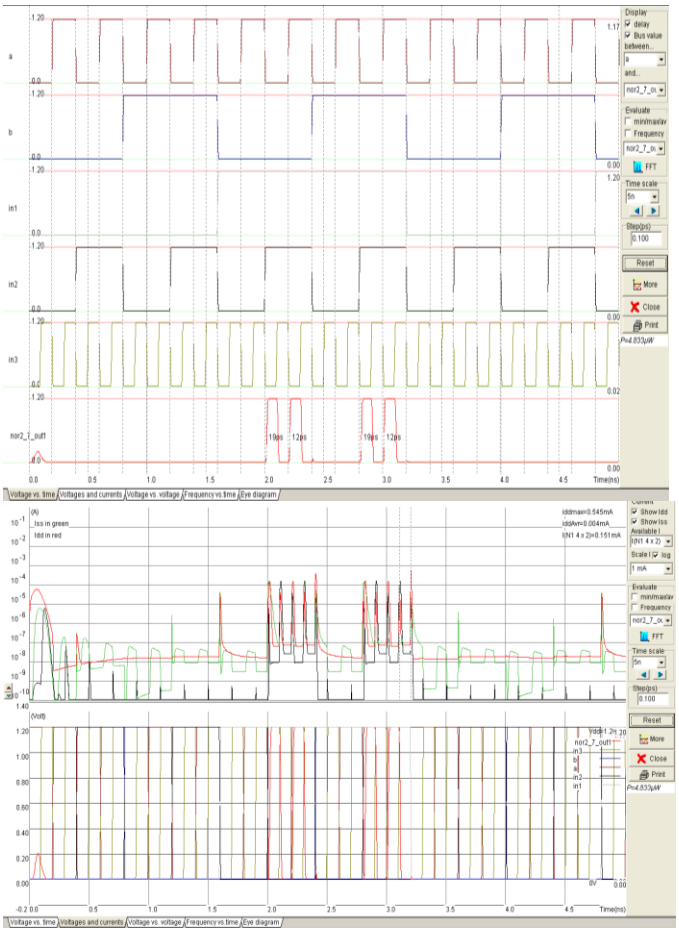


Figure 9.Simulations of Optimized Circuit 1(90 nm).

A. *Results*

Simulations of an unoptimized circuit are shown in Fig. 8. It can be observed from the simulations that glitches are present in the output, which are unwanted transitions and need to be eliminated or reduced. No method to reduce leakage is present in this circuit; due to this leakage current of about 0.215 mA is present as can be observed from waveforms. Glitches present in the O/P and leakage current are major reason here for power consumption.

Simulations of an optimized circuit are shown in Fig. 9. It can be observed from the simulations that glitches are completely eliminated as well as there is a reduction of about 29% in leakage current as observed from the simulations. Because of reduction in leakage current and elimination of glitches, there is a considerable reduction in power consumption. Delay in an optimized circuit is also less as compared to unoptimized circuit.

Simulations for Fig. 6 are shown in Fig. 10 for 250 nm technology. As it can be observed from simulations, glitches are present in the output. Simulations of Optimized circuit 2 shown in Fig. 7 are shown in Fig. 11 for 250 nm technology. Glitches are completely eliminated from optimized circuit's output and considerable reduction in power is also obtained here.

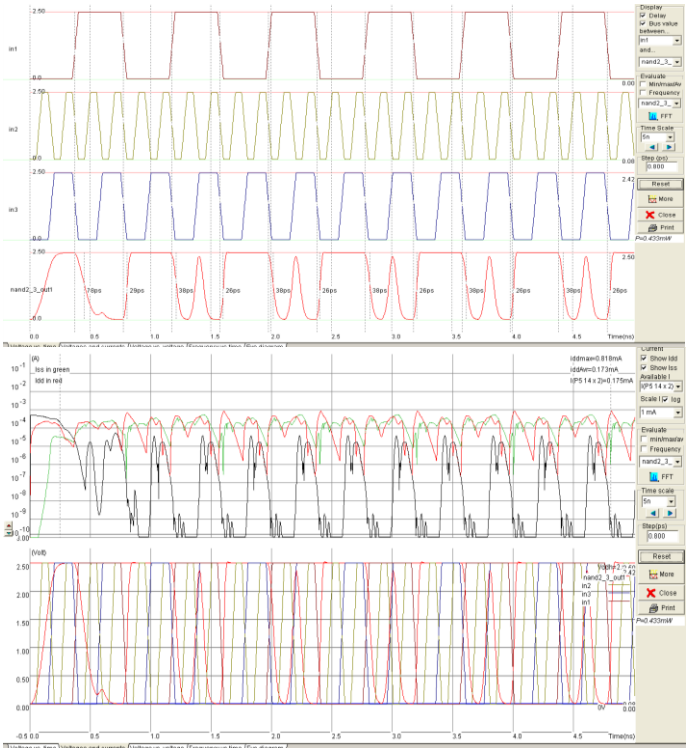


Figure 10.Simulations of Unoptimized Circuit 2 (250nm).

Unoptimized Circuit shown in Fig. 6 is also implemented in 90nm technology and its simulations are shown in Fig. 12.Unwanted transitions are also present here. Due to scaling of technology, the leakage current is also present. Power consumption is due to both the leakage current and these unwanted transitions.

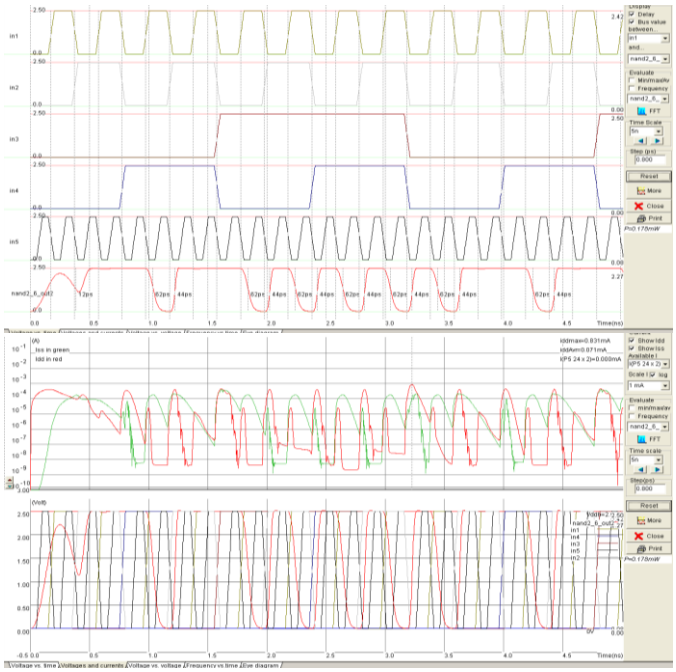


Figure 11.Simulations of Optimized Circuit 2(250 nm).

Simulations of optimized circuit 2 (90 nm) in Fig. 7 are shown in Fig. 13. There is considerable reduction in leakage current as observed from simulations as well as power. But there is little increase in delay of about 1.5ps.

B. Conclusion

Scaling down of the technology has led to increase in leakage current. Nowadays, a leakage power has become more dominant as compared to Dynamic power. But, Dynamic Power consumption due to glitches can't be neglected.

Therefore, in this paper, the efficient technique has been proposed for reducing glitch and leakage power reduction in CMOS VLSI Circuits. The proposed method results in ultra low power consumption.

Two optimized circuits are giving good results in terms of power delay, energy and leakage current as compared to unoptimized circuits. Reduction of about 59.7% is obtained in power and in energy it is 85.28% for optimized circuit shown in Fig. 5 as compared to unoptimized circuit given in Fig. 4.The comparison is shown in Table I given below. The results are simulated using Microwind 3.1 tool in 90nm technology at room temperature for the circuits shown in Fig. 4-5.

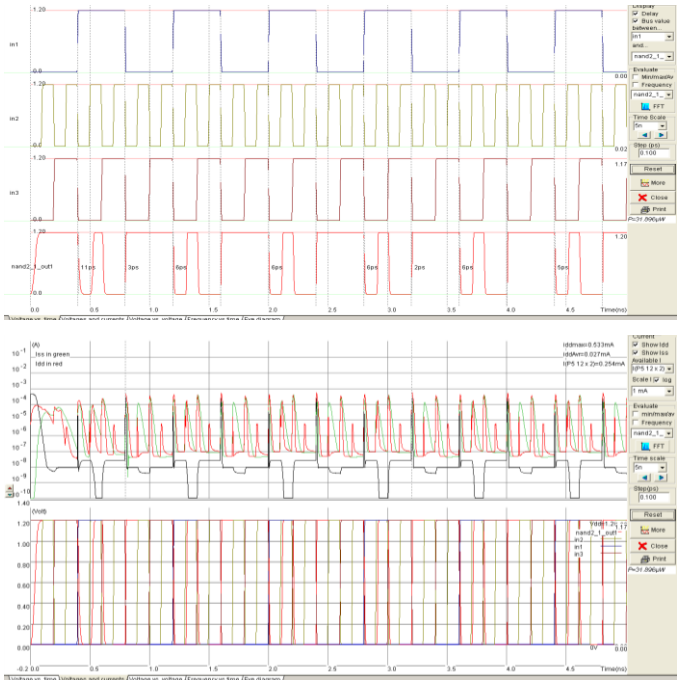
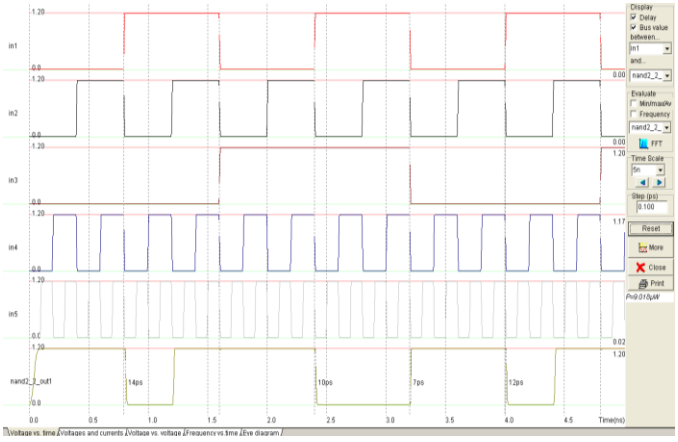


Figure 12.Simulations of Unoptimized Circuit 2 (90 nm).

Circuits shown in Fig. 6-7 are simulated in Microwind 3.1 for both 250 nm and 90 nm technology. Comparison table given in Table II has shown the comparison between unoptimized circuit and optimized circuit 2 for 250 nm technology. An optimized circuit 2 (250 nm) has about 67% energy and 58.8% power reduction as compared to unoptimized circuit 2 (250 nm).

Table III is showing the comparison for 90nm technology.There is about 64.02% energy and 71.72% power reduction in an optimized circuit 2 (90 nm) over unoptimized circuit 2 (90 nm). As it can be observed from results shown in comparison tables, optimized circuits are more energy and power efficient as compared to unoptimized circuits. Glitches are also completely eliminated from outputs of optimized circuits.



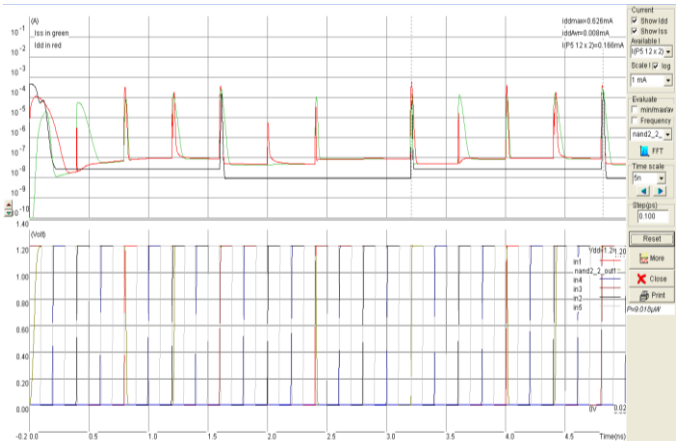


Figure 13.Simulations of Optimized Circuit 2 (90 nm).

TABLE I. COMPARISON BETWEEN UNOPTIMIZED AND OPTIMIZED CIRCUIT 1(90 nm)

Circuit / Parameter	*Unoptimized Circuit 1*	*Optimized Circuit 1*
Power(µW)	11.999	4.833
Delay(ps)	26	9.5
Energy(aJ)	311.974	45.9135
Current(mA)	0.586	0.545
Leakage Current(mA)	0.215	0.151

TABLE II COMPARISON BETWEENNOPTIMIZED AND OPTIMIZED CIRCUIT 2 (250nm)

Circuit / Parameter	*Unoptimized Circuit 2*	*Optimized Circuit 2*
Power(mW)	0.433	0.178
Delay(ps)	39	31
Energy(fJ)	16.887	5.518
Current(mA)	0.818	0.831
Leakage Current(mA)	0.175	0.000

TABLE III COMPARISON BETWEEN UNOPTIMIZED AND OPTIMIZED CIRCUIT 2 (90 nm)

Circuit / Parameter	*Unoptimized Circuit 2*	*Optimized Circuit 2*
Power(µW)	31.896	9.018
Delay(ps)	5.5	7
Energy(aJ)	175.428	63.126
Current(mA)	0.533	0.626
Leakage Current(mA)	0.254	0.166

ACKNOWLEDGMENT

The authors would like to thank Dr. Samir Kumar Das, Director, NITTTR, Chandigarh for constant encouragement and support during this research work. The authors would also like to express their sincere thanks and deep sense of gratitude to Dr. SBL Sachan, Professor and Head, Electronics & Communication Department, NITTTR, Chandigarh for their constant inspirations, guidance and helpful suggestions throughout this research work.

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