Studies and a Method to Minimize and Control the Jitter in Optical Based Communication System

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***Abstract*—In the years, optical communication systems have been using significantly for attractive solutions to the increasing high data rate in telecommunication systems and various other applications. In the present days mostly, two types of communication schemes are using in data communication, namely asynchronous transmission and synchronous transmission depending on their timing and frame format. But both transmission systems are facing complications seriously with the involvement of jitter in data propagation. The jitter can degrade the performance of a transmission system by introducing bit errors and uncontrolled offsets or displacements in the digital signals. The jitter creates problems furiously at high data rate systems. The jitter need to be minimized in the communication system, otherwise it also degrades the performance of the interconnected systems with main circuit. This will happen due to improper synchronization or management of the clock scheme in the communication system. The improper organization of clock scheme propagates fault data and clock scheme to all other interconnected circuits. In the present work a new clock scheme is discussed to minimize the jitter in data propagation.**

Keywords*—Optics; Jitter; pipeline; Clock; propagation delay; high speed data.

I. INTRODUCTION

Traditionally the jitter is measured in Unit Interval, where one Unit Interval corresponds to the phase deviation of one clock period. Controlling jitter is important because jitter can degrade the performance of a transmission system introducing bit errors and uncontrolled errors in the digital signals. Jitter causes bit errors by preventing the correct sampling of the digital signal by the clock recovery circuit in a regenerator or line terminal unit. The more the jitter grows, the smaller the valid bit interval at the end becomes, ultimately producing a higher bit error rate [9].

In optical fibre system the timing jitter generated by noise in the receiver and pulse distortion in the optical fibre. If the signal is sampled in the time between the signal crosses the threshold level, then the amount of distortion ΔT at the threshold level indicates the amount of jitter. Then the Timing jitter is given by,

Timing jitter (%) = $\Delta T/T_b X100\%$

Where, $T_b$is a bit interval
ΔT is the amount of distortion.

Traditionally, the rise time is defined as the time interval between the point where the rising edge of the signal reaches 10 percent of its final amplitude and the time it reaches 90 percent of its final amplitude. However, when measuring optical signals, these points are often obscured by noise and jitter effects. Thus, the more distinct values at the 20 percent and 80 percent threshold points are normally measured [12].

A similar approach is used to determine the fall time. Any nonlinearity of the channel transfer characteristics will create an asymmetry in the eye pattern. If a purely random data stream is passed through a pure linear system, all the eye openings will be identical and symmetrical.

II. METHOD OF TRANSMISSION

In parallel transmission, multiple channels are used to transmit several bits simultaneously, while a single channel is used in serial transmission. Data communication over short distances is generally using serial communication. It reduces the cost effect and complexity in interfacing by implementing single channel for communication. It also needed fewer devices in interfacing. The following parameters needed to consider for smooth transmitting of data over fibre link [12].

A. Line coding

The line coding is required to provide efficient timing recovery, synchronization as and suitable transmitted signal with less distortion. In the present paper optical fibre communications are used and hence large bandwidth is available. So, binary codes are mostly preferred for communication in the present paper. Basically, there are two types of two-level binary level codes that can be used for optical fibre transmission communication links. They are Return-Zero (RZ) and Non-Return-Zero (NRZ) format.

- **Return-Zero Coding (Transmitter)**

In Return to zero communication scheme the voltage levels return to zero after each transmission. In the RZ program, the microcontroller generates two types of clock pluses. One of the clock pulses is required for the shift register to serialize the parallel input from the USB module, another clock pulse is for

the RZ module. The ratio of Shift register clock pulse to RZ clock pulse is 1:2.

- **Return Zero (Receiver)**

When the microcontroller detects the stop bit at the end of each byte, it will then generate 2 types of clock pulse. The first would be used to "push" the signal into the RZ circuit in which it will convert RZ signal into NRZ waveform. The second clock pulse will be used to read the signal from the serial to parallel shift register.

- **Non-Return-Zero Coding (Transmitter)**

The transmitter microprocessor consists of two programs, RZ and NRZ module. In the NRZ program, the microcontroller generates a type of clock pulse that is being used for shift register to serialize the parallel input from the USB. The serialize data is then feed to the data line for transmission. The transmitter signal is the same as the signal generated out from the shift register.

- **Non-Return-Zero Coding (Transmitter)**

When the microprocessor detects a start bit, it will start to tickle the shift register. The time duration for each clock pulse is approximately one micro second, which is approximately the same clock pulse, generated by the transmitter's clock. Thus one clock pulse is needed for the shift register to record in the data. After collecting all the 8 bits data, the microprocessor would finally generate a clock pulse to input the data from shift register to the computer via USB module.

B. Data communication scheme

Currently, two types of communication schemes are used in data communication. They are asynchronous transmission and synchronous transmission depending on their timing and frame format.

- **Asynchronous Transmission**

In asynchronous transmission, the transmitter and receiver clocks are free-running and are set to approximately the same speed. A start bit is transmitted at the beginning of each character, and at least one stop bit is sent at the end of character. The stop bit leaves the line or channel in the mark condition, which represents binary 1, and the start bit always switches the line to a space (binary 0). The timing remains accurate throughout the limited duration of the character as long as the clocks at the transmitter and receiver are reasonably close to the same speed. There is no set length of time between characters in asynchronous transmission. The receiver monitors the line until it receives a start bit. It counts bits, knowing character length being employed, and after the stop bit, it begins monitor the line again, waiting stop bit [13].

- **Synchronous Transmission**

In synchronous transmission, the transmitter and receiver are synchronized to the same clock frequency. As start and stop bits are not necessary, synchronous communication is more efficient than asynchronous and block of data is sent, that are much longer than a single character. Blocks begin with an identifying sequence of bits that allows proper framing and often identifies the content of the block. Synchronous transmission is more difficult and more expensive to implement than asynchronous transmission. It is used with higher transfer rates of communication: Ethernet etc. It is used in fast transfer rates (100kps to 100Mbps) [13].

The simplest solution for inter-domain data transfer is the two-flip-flop synchronizer [3]. The main problem with that synchronizer is its low throughput: typically, a complete transfer incurs waiting about one to two clock cycles at each end, and the next transfer cannot start before that handshake is complete. Although it is a very robust solution, it is sometimes misused or even abused in an attempt to reduce its latency [4][5].

In high-speed applications, logic channels are sometimes used as un-clocked information pipelines (e.g. wave pipelining), either to avoid distributing high-frequency clocks or to accommodate large delays (e.g. off-chip drivers) where synchronous pipelining is expensive or impractical [1][2]. In these circuits the quality is

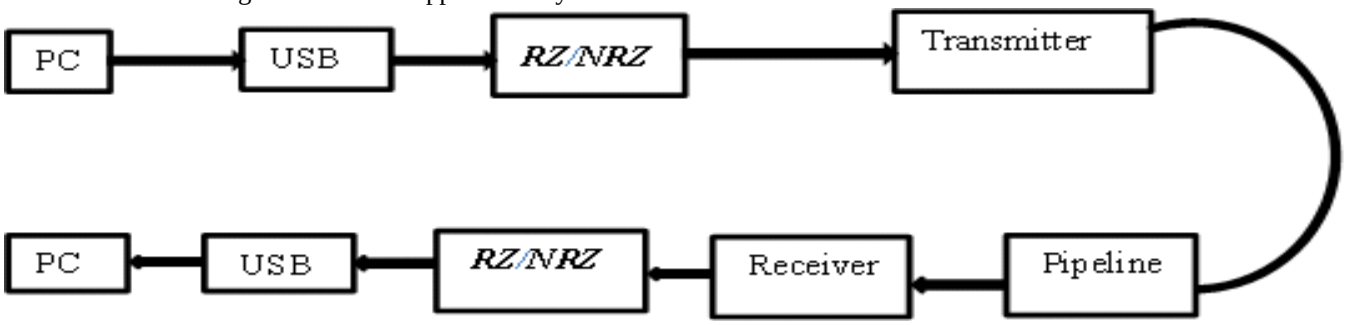

Fig.1. Block Diagram Optical Communication System with new method including pipeline.

determined by clock skew and jitter [9]. In the conventional pipeline system, it is facing problems due to improper synchronization of clock pulses. This is a universal problem in all the digital systems mostly called clock skew. The system clocking must be such that the output data is clocked after the latest data has arrived at the outputs and before the earliest data from the next clock cycle arrives at the outputs [8].

In this crucial period it is difficult and highly impossible to get exact input data match with the output in conventional circuits. The problem can be solved with new clock scheme [8]. In the present paper same clock scheme with more intelligent system is adopted. In this new method, after arriving of first valid data at interrupt controller the interrupt controller interrupts microcontroller. In response to this interrupt the microcontroller send a clock signal to the next stage register.

Similarly after receiving a valid signal from second register the interrupt controller again interrupts the microcontroller. The microcontroller in the same way activates the next stage in a different path [10][11].

III. MOTIVATION

In any Interfacing system the data must be fed to processor at exact clock pulse. If the handshaking does not exist between two processor and transmitter, there may be a chance of data loss. It leads degradation in accuracy [11]. For example in figure 1 if the transmitter speed is high than the receiver system, the receiver may loss some data. This is due to speed miss-match between transmitter and Receiver. There are some methods effectively acting to minimize these data losses using new pipeline techniques [11][10]. The new clock schemes and constraints in the new pipeline systems are described in the past methods [10]. In the present paper the new clock scheme is interfaced between transmitter and receiver to minimize the jitter.

IV. EXPERIMENTAL SETUP

An USB is used to interface the transmitter for fast and simple interface. The RZ and NRZ circuits are used in communication to minimize the power consumption and length of sampling time. Figure 2 is showing Return Zero (RZ) and Non-Return Zero module used for transceiver communication. A detailed description of outputs and operations are discussed in the next section. The inputs of various ranges are produced by function generator, to feed the circuit as shown in figure 2. The inputs are feed to RZ /NRZ circuits through USB. An optical fiber is connected for data transmission. The optical fiber is used as channel to carry the data pulses to satisfy the operations through transceiver. Optical fiber is selected in the present work because of its vast advantage in tele-communication system. Optical fiber supports fast data transmission rates. But it generates jitter due to noise at receiver side and due to the distortion in the fiber. A two stage pipeline is interfaced between transmitter and receiver to minimize the jitter and data losses.

Advantages of Optical Fiber: Some of the advantages are discussed in the present section.

a) In the long distance communication the network connection is more flexible and transmission errors are almost zero.

b) Fiber cable support higher data rates. That is why, in the present work a pipeline technique is used to synchronize the transmitter with receiver.

c) Fiber cables have long life time when compare with copper wires. They are more reliable than any other channel.

d) Fiber cables are resistible to cross talk and Electro Magnetic Interferences.

e) They are easier to test and interface.

f) Installation costs of fiber cables are cheaper than other channel installations.

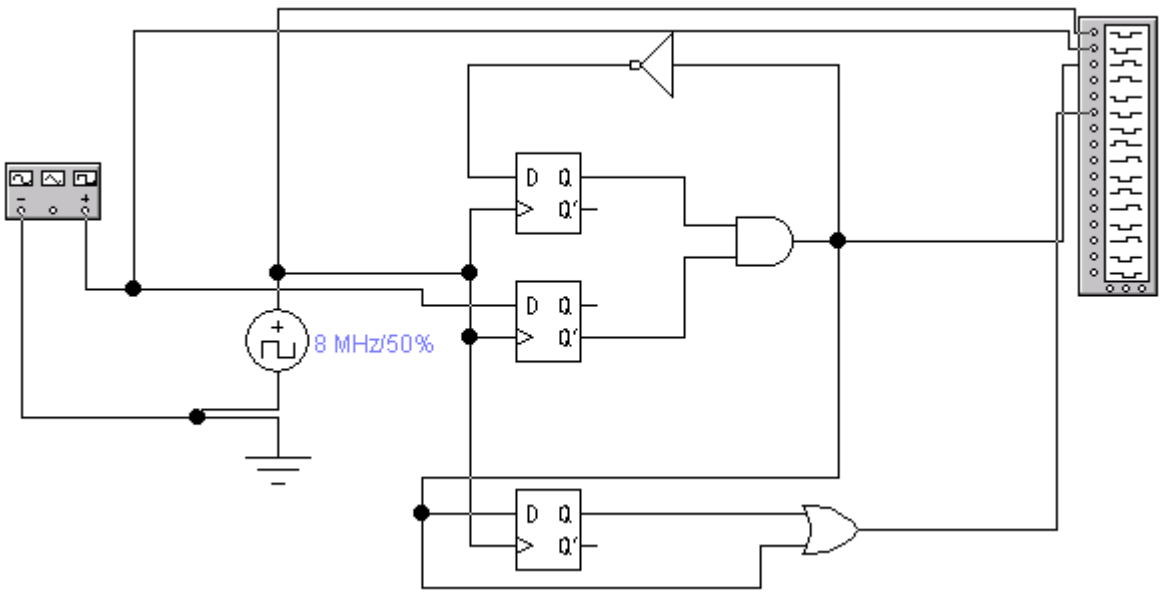

Fig.2. Analysis Circuit of Return Zero Transmitter and Receiver Module

V. RESULTS

In figure 3 and figure 4 the first wave showing the clock pulse applied to the circuit. The second pulse is generated from function generator given as input data to RZ and NRZ circuit. The red line and blue vertical lines are representing the width of the pulses. The outputs are generated and analysed in Electronic work bench and Proteus. The circuit is analysed for various ranges of input data rates [11] and taken screen shots as shown in figure 3 to figure 7. The Digital circuit is studied without pipeline and then after compared the operation by integrating with pipeline in the circuit.

At higher data rates, due to noise and jitter some distortions are observed as shown in figure 6. By interfacing the new pipeline module some distortions are minimized, which is shown in figure 7. In figure 6 and figure 7, the yellow pulse represents the first stage clock pulse and blue line represents the second stage clock pulse. The pink pulse represents the data output of the optical fiber and green colour represents the data output at the receiver. Figure 6 is the simulated output of the circuit without pipeline and figure 7 is the simulated output of the circuit with pipeline.

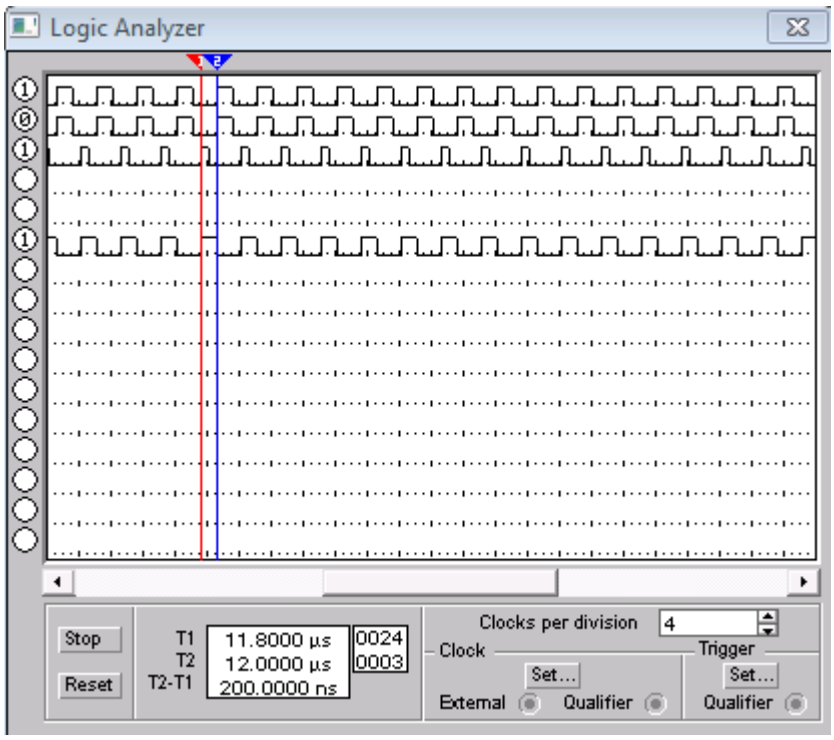

Fig.3. Logic Analyser of Return Zero Transmitter and Receiver Module with 2MHz input

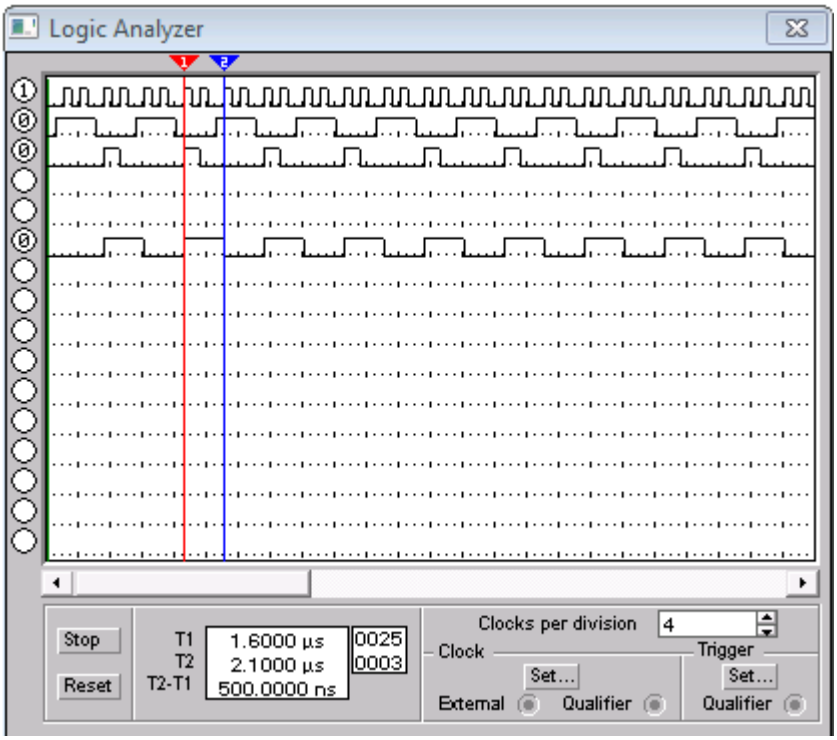

Fig.4. Logic Analyser of Return Zero Transmitter and Receiver Module with 1MHz input

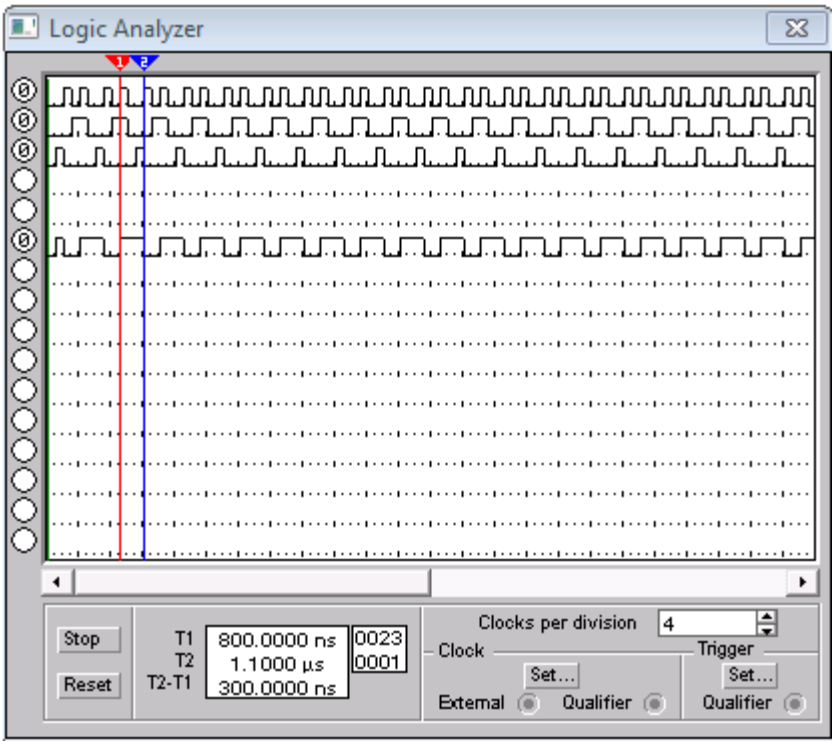

Fig.5. Logic Analyser of Return Zero Transmitter and Receiver Module with 8MHz input

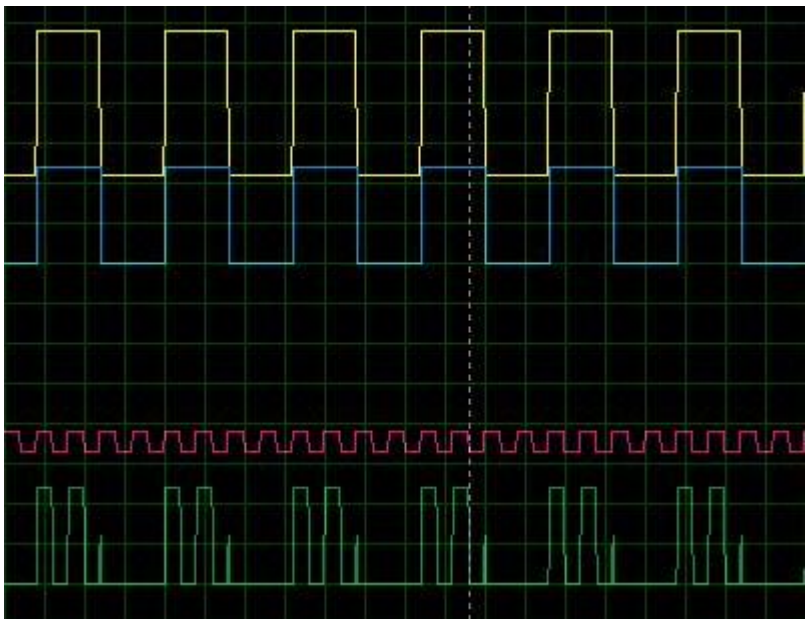

Fig.6. Logic analyser of Optical communication system without pipeline

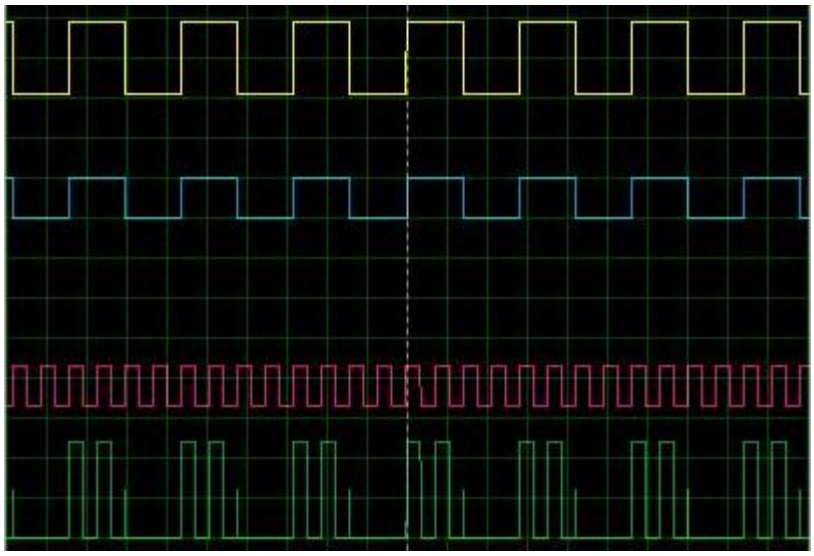

Fig.7. Logic Analyser of optical communication system with new pipeline system

At higher frequency rates the RZ receiver is unable to produce the desired output. At high frequencies the pulse width is more when compared with low frequency rate receiver module. This deviation produces distortion at receiver. In the present work a new pipeline technique is discussed to minimize jitter at receiver side. A new pipeline technique [1] is interfaced between optical system and receiver RZ module.

VI. CONCLUSION

Jitter can degrade the performance of the fibre-optic system by causing bit errors. The faster and more complex the system becomes, management of jitter is increasingly critical. This is because; at higher data rates bits are placed more closely together. In the present work the jitter minimization techniques are discussed to improve the system performance at wide range of data rates. The system is clocked such that a pipeline stage is operating on more than one pulse simultaneously. The present system at any given time, multiple pulses can be present in a stage.

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Biography

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