A Novel Neural Network Based Method Developed for Digit Recognition Applied to Automatic Speed Sign Recognition

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Abstract—This Paper presents a new hybrid technique for digit recognition applied to the speed limit sign recognition task. The complete recognition system consists in the detection and recognition of the speed signs in RGB images. A pretreatment is applied to extract the pictogram from a detected circular road sign, and then the task discussed in this work is employed to recognize digit candidates. To realize a compromise between performances, reduced execution time and optimized memory resources, the developed method is based on a conjoint use of a Neural Network and a Decision Tree. A simple Network is employed firstly to classify the extracted candidates into three classes and secondly a small Decision Tree is charged to determine the exact information. This combination is used to reduce the size of the Network as well as the memory resources utilization. The evaluation of the technique and the comparison with existent methods show the effectiveness.

Keywords—Image processing; Road Sign Recognition; Neural Networks; Digit Recognition

I. INTRODUCTION

Nowadays, intelligent driver assistance systems stand as an important component in new vehicle generation. These systems assist the driver in many driving situations and contribute to decreasing the risk of accidents. Artificial perception modules are used to develop various and different driver assistance tasks. Vision-based modules are involved in many types of research in this topic. Numerous assistance applications were exploited such as automatic obstacle avoidance, vehicle detection and recognition, line following, traffic lights detection and many others. This work, deals with the development of an intelligent vision-based system to recognize speed limit signs. In purpose to achieve real-time processing constraints, the complete image processing system is decomposed into sub-processing levels. This paper discusses a new method developed for the identification of the speed limit value. The main goal consists in recognizing the nature of the interior symbol: whether it is a positive speed value candidate and so identifying the exact value or not a speed value candidate. The input data for this task is a small binary image presenting the pictogram extracted from a detected circular road sign with a red border. A detection process precedes the recognition one to detect and extract this type of road signs. The speed limit recognition problem can be addressed as a digit candidate identification which is the subject of this work. The developed approach uses as a first step a Neural Network that classifies the detected candidates into three classes and as a second step a small Decision Tree is used to identify the exact information: a positive digit candidate and so gives the value or a negative candidate. The main contributions proposed in this work consist in reducing the Neural Network architecture and the development of a technique that is well-suited for real-time processing and hardware implementation.

The remainder of this paper is organized as follows: In Section II, a review of previous work is presented. The proposed method is discussed in Section III, whereas the performance evaluation is proposed in Section IV. Concluding points and future work are drawn in the conclusion.

II. RELATED WORK

The majority of existing automatic road sign classification and recognition, as well as candidate identification especially digit candidate use artificial intelligence based algorithms. Many issues have involved Support Vector Machine (SVM) in the recognition stage. Arroyo et al [1] have proposed a method based on SVM to classify signs according to their geometric shapes. Authors in [2] have also used SVM to classify road signs based on shapes. A group of cascade SVM classifiers was used in [3] to classify detected road signs. A new method for pictogram classification was presented in [4] using Decisiontree-based support vector multi-class classifiers. Authors in [5] have used self-organizing maps for the detection and recognition of road signs. In the recognition stage, the nature of information is identified using the distribution of dark pixels in the pictogram of the detected sign. Neural Networks have also been involved in various recognition tasks [6-9]. In [10] a Neural Network was designed to recognize traffic sign patterns. In purpose to minimize the number of input units from 2700 units that presents the number of all pixels in the three channels R,G and B of the detected pictogram to a reduced number, they calculate three normalized averages, 30 inputs from the vertical histogram and 30 inputs from the horizontal histogram. These 63 parameters present then the total input units of their designed Network. Maurice et al [11] have used Convolutional Neural Networks for speed signs recognition. The input layer is composed of 32x32 units presenting the pixels of the extracted pictogram. The

recognition of the speed value presents a challenging problem among these researches. There are issues that use the detected sign matrix as input to the recognizer [12]. Others consider the extracted pictogram matrix as input [11]. In [13] the binary matrix of the first extracted digit is used, whereas in [14] authors prefer to recognize each extracted candidate separately. In spite of the many advantages shown by Neural Networks in recognition problems due to their high learning capabilities, the real-time processing and memory resources utilization is related to the complexity and the architecture of the designed Network. One of the key points that well contribute to simplify the architecture is reducing the number of input units. This research interest the conception of a simple and performing technique for digit candidate recognition applied to speed sign recognition. The proposed method is presented in the next section.

III. PROPOSED METHOD

This section describes the developed digit recognition technique. This technique is part of a complete recognition system which is developed for rounded speed limit signs with red border detected on an RGB image. The detection stage allows detecting this type of signs and extracting the first character of the interior information which can be the first digit of a speed value or another type of information. The extraction step is presented in Fig. 1. Where (a) is the detected circular road signs in the RGB image. The size of this extracted pattern is not fix for different images, for this example the size is 33x33. A resizing is applied then to all detected signs to normalize the size to 32x32. (b) is the Red component of the resized sign. (c) is the result of converting (b) to binary image using a simple thresholding method. (d) is the first character extracted from (c). The size of (d) is 32xM where M is a scalar less than or equal to 32.

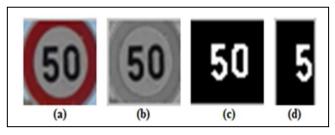


Fig. 1. Digit candidate extraction from a detected sign

The use of Neural Networks in the recognition stage for this application was investigated in many researches. Authors in [15-16] have developed Networks were the input layer consists in the extracted digit pattern. The total number of input neurons is equal to the total number of pixels. Respectively 400 pixels (20x20) for [15] and 72 pixels (6x12) for [16]. The use of a large number of input units requires more computation time and more memory resources. A simple method that reduces the number of inputs and uses a simple Neural Network architecture was tried and developed. The technique is divided into two parts: In the first one a Neural Network is designed to determine the class of the digit candidate from three probably classes. Then in the second part a small Decision Tree is charged to recognize the exact signification (a number from 0 to 9 or not a number). The number of units in the input layer is equal to 11 units. These input values are extracted from the digit candidate binary image. The realization of the recognition task is described in the following steps.

A. Neural Network creation

This section describes the different steps achieved in the design of the Network architecture. The used Net is a feedforward multi-layer Network.

A pretreatment is carried on the binary image of Fig. 1 (d) to extract parameters to be used as the Network input.

As shown in Fig. 2 a left projection of the candidate image is done to calculate at each row the distance to the first foreground pixel.

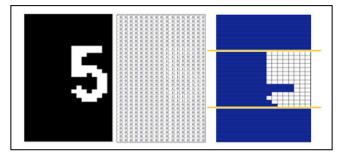
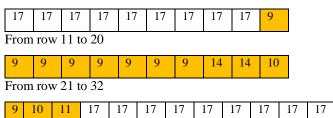


Fig. 2. Left projection and distance calculation

An array of 32 distances 'dis' is obtained as follows:

From row 1 to 10



This array is used to fill the 'dr' array consisting in the 11 Neural Network inputs as described in TABLE I, where D₋₁, D₀ and D_1 present the difference between two consecutive distances. If these distances are equal then the 'dr' case corresponding to D_0 is incremented. D_{-1} is incremented if the left distance is greater than the right one and D_1 is incremented in the opposite situation. Only the part containing the digit is considered for which the corresponding distances are marked in orange color. Fig. 3 explains the idea. The following array describes the obtained input array of the preceding example.

The Pseudo-code of the process is exhibited as follows:

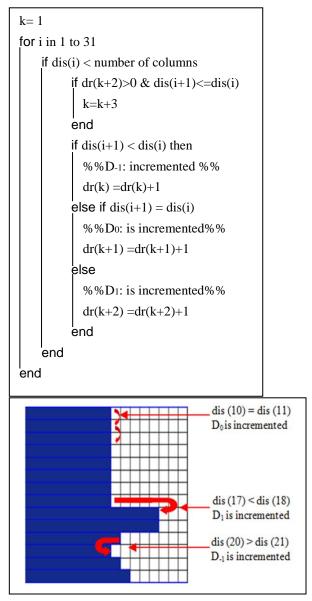


Fig. 3. Process to fill the input array

Fig. 4 shows extracted digit candidates for numbers varing from 0 to 9. These candidates are extracted from detected road signs in road images. TABLE I exhibits the corresponding Neural Network input arrays determined as explained previously for these candidates. The analysis of a large number of extracted digits have shown that using this input vector allows to classify them into three classes. The first one is including 1,2,4 and 7, the second one is including 0 and 6 and the third class includes 3,5,8 and 9. The designed Neural Network is charged to determine the class of the digit candidate. But given that the detection module can detect not only speed signs but some other signs can be detected due to their rounded geometry and red border like in Fig. 5, the separated characters of the detected pictogram are extracted and processed seperately to guarantee the accuracy of the method.

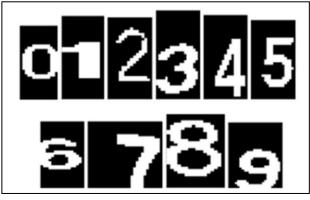


Fig. 4. Examples of extracted digit candidates



Fig. 5. Other circular road signs with red border

Value	NN input array 'dr'
0	37101200000
1	2110900000
2	4 1 1 7 7 0 0 0 0 0 0
3	41121221300
4	71010300000
5	19113101200
6	2102000000
7	04251400000
8	32102226101
9	44422200000

 TABLE I.
 CORRESPONDING NN INPUT VECTORS RELATED TO SAMPLES OF FIG. 4

The final Neural Network (NN) architecture is shown in Fig. 7. The input layer is composed of 11 neurons. The output layer consists of two neurons presenting the candidate class as follows:

class 1: 0 0 (1,2,4,7) class 2: 0 1 (0, 6) class 3: 1 1 (3,5,8,9)

The number of hidden layers and hidden units was fixed after empirical training of the Network changing the training and transfer functions and other parameters. The final architecture was fixed when desired mean-squared error was reached taking into account reducing the network complexity. In purpose to simplify the hardware implementation of the designed system the elliot symmetric transfer function [17] was used in this work. This function is defined by equation 1. Its main advantage that is suitable for hardware implementation. Contrary to other sigmoid function, it does not require the implementation of any exponential function which requires high memory resources in hardware implementation.

$$\text{Elliotsig}(\mathbf{x}) = \frac{\mathbf{x}}{1 + abs(\mathbf{x})} \tag{1}$$

Fig. 6 shows the comparison between the hyperbolic tangent sigmoid transfer function and elliot symmetric one.

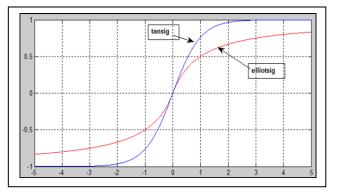


Fig. 6. Hyperbolic tangent sigmoid transfer function $Vs\ Elliot$ symmetric one

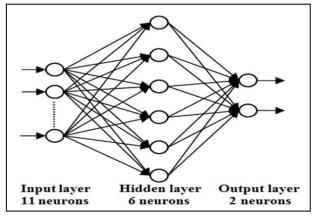


Fig. 7. Final architecture of the Neural Network Classifier

TABLE II. NEURAL NETWORK EVALUATION

Class	Total samples	Correct classification	Classification %
1	69	67	97.10 %
2	34	31	91.18 %
3	65	61	93.85 %

B. Decision Tree realization

The second part of the recognition system is accomplished with a small Decision Tree (DT) shown in Fig. 8. This DT is designed to determine the nature of the extracted candidate firstly classified with the NN. Some parameters are used in the DT which are shown in Fig. 9 and are respectively:

Nbi: Presents the number of intersection of the ith column with the character, where the ith column contains the center of geometry.

Dr(1) is the value of the first value of the "**dr**" array.

Nbt : Presents the maximum difference between two consecutive distances where the right one is greater than the left one.

b: Presents the number of consecutive zeros in the central column below the central pixel.

h: Presents the number of consecutive zeros in the central column above the central pixel.

ND: Means Not a digit.

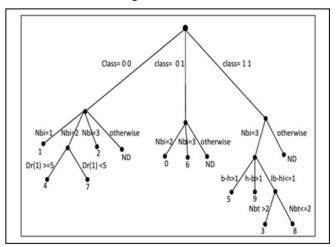


Fig. 8. Architecture of the Decision Tree

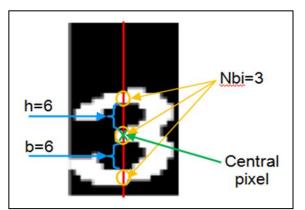


Fig. 9. Extraction of the different parameters

IV. EVALUATION

Fig. 10 shows the complete recognition process where Nc is the number of separated characters in the extracted pictogram. Given the binary matrix of the extracted first digit candidate, NN inputs are calculated and passed throw the network for the first classification. Then the DT is charged to identify whether it is a positive or a negative digit candidate.

The second character is then processed similarly if the first candidate is identified as a positive digit candidate to obtain the final decision.

If the information contains only one symbol it will be rejected and decided as no speed sign given that a speed value should be composed of 2 or 3 separate characters. TABLE III presents different Network architectures and their relative mean-squared error. TABLE IV presents the classification results carried on a number of testing images for the best Network architecture, the one with one hidden layer and 6 hidden units. This table exhibits the classification percentage for the NN and the DT separately and then for the whole system.

TABLE V shows the performance comparison of the proposed method with the method discussed in [16].

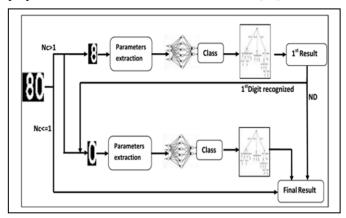


Fig. 10. Speed value recognition process

TABLE III. NETWORK ARCHITECTURES

NN Architecture	Mean Squared error
11-5-2	0.0980
11-6-2	0.0298
11-7-2	0.0777
11-8-2	0.1115
11-10 - 2	0.1081
11-12 - 2	0.0811
11-10 - 7 -2	0.0473
11-13 - 5 -2	0.0541

Proposed Method					
NN	DT	NN+DT			
94.64%	98.55%	93.45%			

TABLE V. PERFORMANCE COMPARISON

	Architecture	Total signs number	Recognition %
This work	NN+DT 11-6-2	168	93.45%
Method in [16]	NN 72 - 10 -10	128	82.8%

TABLE IV shows the classification rate of the proposed method carried on a 168 testing samples. The recognition percentage of the DT is the percentage of the correct recognized samples among the 159 correct classified samples by the NN. These results show the robustness and accuracy of the developed method. TABLE V exhibits the advantages of the method compared to [16]. The developed technique gives a high recognition rate with simple and soft architecture.

V. CONCLUSION

This paper has presented a new, robust and efficient approach to identify positive digit candidates extracted from detected road signs. The main advantages of this work consist in the simplicity of the Network architecture and the short computation time. Compared to approaches [12, 13, 15, and 16] in which an important number of input units was used that complicate calculations and require a high number of hidden neurons. The use of the DT as a complementary task didn't complicate the system. Indeed it is composed of a minimum number of branches and leaves that require a very short computation time. In order to minimize the hardware implementation of the designed system the Elliot symmetric transfer function is used in the NN. This function requires simple hardware calculations contrary to other sigmoid functions that need high memory resources to implement exponential and other geometric functions. The recognizer discussed in this paper presents a part of a complete intelligent speed sign recognition system that is designed to be implanted on an FPGA hardware architecture in future works.

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