A Reduced Switch Voltage Stress Class E Power Amplifier Using Harmonic Control Network

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***Abstract*—In this paper, a harmonic control network (HCN) is presented to reduce the voltage stress (maximum MOSFET voltage) of the class E power amplifier (PA). Effects of the HCN on the amplifier specifications are investigated. The results show that the proposed HCN affects several specifications of the amplifier, such as drain voltage, switch current, output power capability (C_p factor), and drain impedance. The output power capability of the presented amplifier is also improved, compared with the conventional class E structure. High-voltage stress limits the design specifications of the desired amplifier. Therefore, several limitations can be removed with the reduced switch voltage. According to the results, the maximum drain voltage for the presented amplifier is reduced and subsequently, the output power capability is increased about 25% using the presented structure. Zero-voltage switching condition (ZVS) and zero-voltage derivative switching condition (ZVDS) are assumed in the design procedure. These two conditions are essential for high efficiency achievement in various classes of switching amplifiers. A class E PA with operating frequency of 1 MHz is designed and simulated using advanced design system (ADS) and PSpice software. The theory and simulated results are in good agreement.**

Keywords*—class E power amplifier; harmonic control network (HCN); MOSFET drain Impedance; ZVS and ZVDS conditions

I. Introduction

The main blocks in many communication systems are power amplifiers. Power amplifiers are high-consumption elements, and so, their efficiency is an important factor in the design procedure [1-3]. Class E power amplifiers are very interesting for communication systems due to their high efficiency. Class E amplifiers are also called DC-AC inverters, which are further divided into two main types: the ZVS power amplifiers and the zero current switching (ZCS) power amplifiers. Both ZVS/ZVDS conditions must be considered in the nominal operation of ZVS type amplifiers, while in sub-nominal operation only ZVS condition is considered. The ZVS type class E PA with nominal operation is studied in this paper. Several researches have been mentioned ZVS and ZVDS conditions as essential conditions to obtain high efficiency in high frequencies [4-6].

Recently, extra parameters have been assumed in some approaches to add one degree of freedom to class E PA design. For example, the shunt intrinsic capacitance (C_{ds}) of the MOSFET is considered nonlinear, and the grading coefficient is taken into account as a new parameter in class E amplifier design [7-8]. Besides, input voltage duty cycle is considered to analyse the class E PA in [9-11]. Varying input voltage duty cycle leads to change in the class E PA specifications. Also, recent approaches have introduced several structures with improved MOSFET voltage and current waveforms, such as inverse class E [12-14], class EF [15-17], and class DE power amplifiers [18-19]. Class DE amplifiers are introduced by adding two parallel capacitances to the switching MOSFETs. Class DE amplifiers have high efficiency, but their output power capability (C_p) is low. Inverse structure of class E is similar to typical structure, but has a dual circuit. ZCS and ZCDS (zero current derivative switching) conditions could be satisfied in Inverse type of class E PA. Combining the structures of class E and F PAs leads to class EF family amplifiers. Reduced switch (MOSFET) voltage or current could be achieved in this kind of amplifiers, according to the harmonics effects on the MOSFET voltage and current, while their efficiency is low, compared with the other switching classes. The ZVS and ZVDS conditions could also be satisfied in the class EF family amplifiers.

In comparison with the mentioned structures, the class E PA has high drain efficiency; however, its C_p factor is low. Therefore, increasing the C_p factor and decreasing the voltage stress in class E amplifier, are still subject to interest. In this paper, a harmonic control network (HCN) is designed and applied in the typical class E amplifier circuit to reduce the maximum value of the MOSFET voltage and also to improve the C_p factor of the amplifier.

The paper sections are summarized as follows. Sections II and III present the structure and specifications of the typical class E PA. Description of the presented HCN and C_p factor of the presented PA are described in Sections IV and V, respectively. Obtained results of the design examples are given in Section VI. Finally, the conclusions of the obtained results are presented in Section VII.

II. Typical Class E PA Structure

The typical class E circuit is depicted Figure 1, which includes a transistor (MOSFET) as a switch, RF choke, series resonator, dc supply voltage (V_{dc}), and a parallel capacitance. The parallel capacitance (C_{sh}) in class E PA includes the MOSFET intrinsic capacitance (C_{ds}) and a shunt external capacitance. However, the external capacitance could be neglected to reach higher operating frequency.

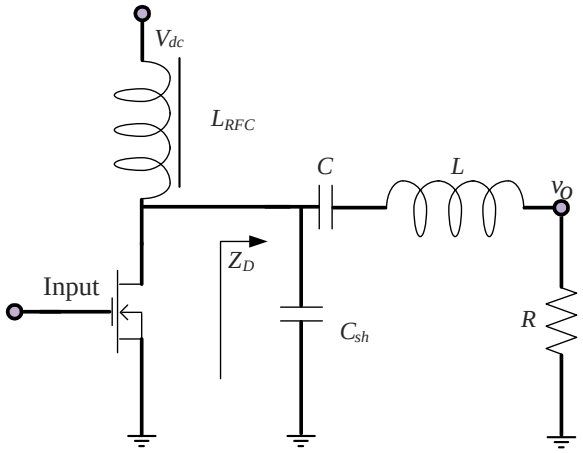

Fig. 1. Typical class E circuit

The normalized MOSFET voltage (v_s/V_{dc}) and normalized MOSFET current (i_s/I_{dc}) waveforms of a typical class E structure are illustrated in Fig. 2. According to this figure, the maximum values of v_s/V_{dc} and i_s/I_{dc} for typical class E amplifier are 3.56 and 2.86, respectively. According to breakdown voltage constraints of the MOSFET, V_{dc} and subsequently the output power could not exceed from a specific value and this problem limits the design procedure. With reduced maximum switch voltage, more output power could be achieved, and the design process of the presented structure would be more flexible.

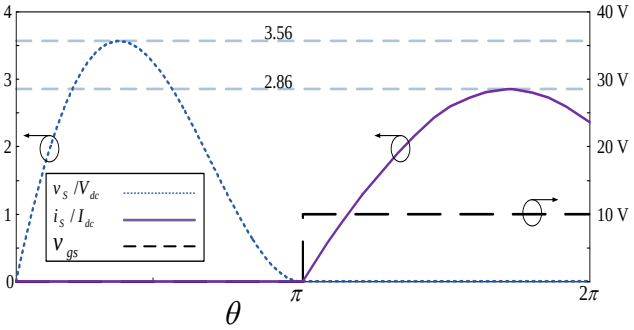

Fig. 2. v_s/V_{dc} and i_s/I_{dc} waveforms of the typical class E structure

III. Drain Impedance

In class E structure, the MOSFET plays the switch role in the circuit and threshold voltage (V_{th}) acts as a trigger for this switch. It means when the input voltage value is higher than V_{th}, the switch (MOSFET) is on, and the value of v_s is equal to zero. On the contrary, when the input voltage value is lower than V_{th}, the switch (MOSFET) is off, and the switch voltage can be calculated, according to the amplifier circuit. The obtained switch voltage waveform of class E amplifier depends on the drain impedance (Z_D). According to Fig. 1, the value of Z_D, can be calculated as follows

$$Z_D = \frac{LCS^2 + RCS + 1}{LCC_{sh}S^3 + RCC_{sh}S^2 + (C + C_{sh})S}. \quad (1)$$

As can be seen in equation (1), the value of Z_D is a function of L, C, C_{sh}, R, loaded quality factor (Q) and frequency. From equation (1), the value of Z_D for the typical class E PA output structure could be achieved, which is depicted in Fig. 3. The drain impedance of the typical structure has a zero and a pole near the operating frequency.

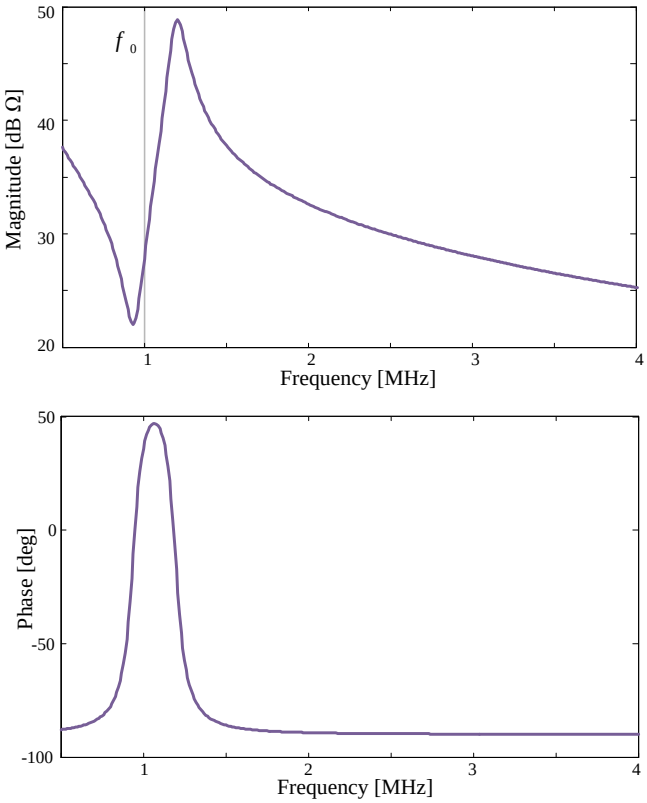

Fig. 3. The value of Z_D for the typical class E output structure

In the circuit structure, high value of Q for the resonant circuit provides a pure sinusoidal voltage at v_o. The value of loaded quality factor could be written as

$$Q = \frac{\omega L}{R}, \quad (2)$$

where ω is angular frequency. Effect of different values of Q on drain impedance is shown in Fig. 4. According to this figure, as the loaded quality factor increases, the zero and pole of the impedance become closer to operating frequency, and the ideal resonator will be achieved with a high value of Q.

IV. Harmonic Control Network

As mentioned, the class E PA drain voltage depends on the drain impedance. It means the switch voltage can be reduced using harmonic control elements. A harmonic control network is designed and inserted in typical class E circuit to decrease the MOSFET voltage. The proposed HCN structure includes two resonator branches, as illustrated in Fig. 5. The circuit values of the designed circuit are tabulated in Table 1.

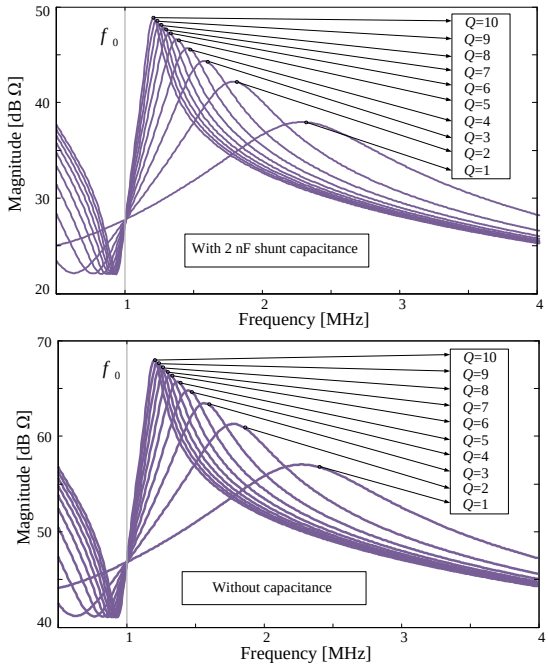

Fig. 4. Effect of Q on the typical class E PA drain impedance with and without shunt capacitance

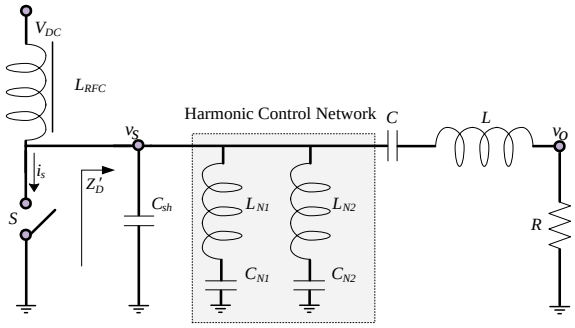

Fig. 5. Proposed harmonic control network in the amplifier circuit

The impedance of the HCN could be written as

$$Z_{HCN} = \frac{L_{N1}L_{N2}C_{N1}C_{N2}S^4 + (L_{N1}C_{N1} + L_{N2}C_{N2})S^2 + 1}{C_{N1}C_{N2}(L_{N1} + L_{N2})S^3 + (C_{N1} + C_{N2})S}. \quad (3)$$

The impedance of the HCN is illustrated in Fig. 6. There is a zero in the impedance of the presented HCN in the third harmonic of the operating frequency. According to Fig. 5, the drain impedance of the proposed amplifier is

$$Z'_D = Z_{HCN}\frac{LCS^2 + RCS + 1}{F(S)} \quad (4)$$

where $F(S)$ is defined as

$$F(S) = Z_{HCN}LCC_{sh}S^3 + (LC + Z_{HCN}RCC_{sh})S^2 + (Z_{HCN}(C + C_{sh}) + RC)S + 1 \quad (5)$$

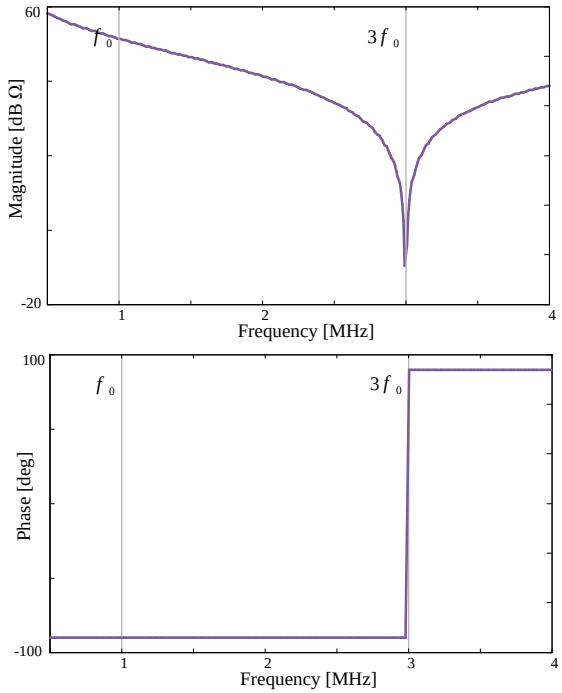

Fig. 6. Impedance of the presented HCN

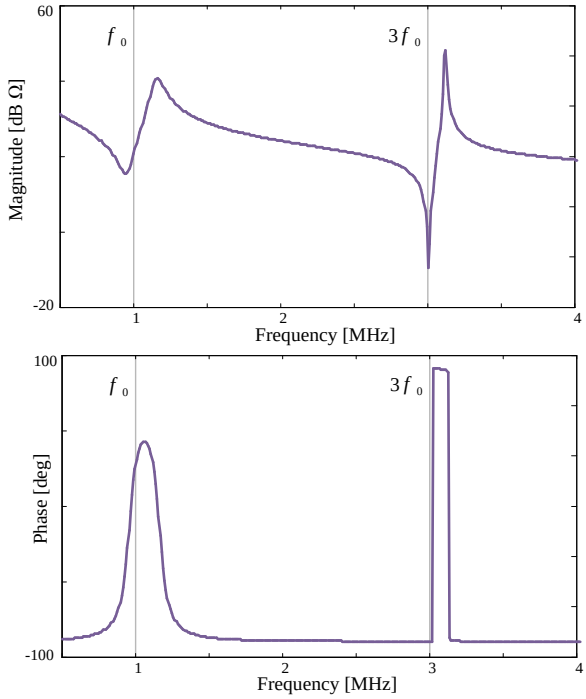

Fig. 7. Drain impedance of the presented amplifier using the proposed HCN

The drain impedance of the presented amplifier using the proposed HCN is shown in Fig. 7.

V. Output Power Capability

To compare the output power of different amplifiers, the output power capability (c_P) factor is used. The c_P factor could be calculated as follows [20]

$$c_P = \frac{P_{o,\max}}{v_{s,\max} i_{s,\max}} = \frac{1}{\frac{v_{s,\max}}{V_{DC}} \frac{i_{s,\max}}{I_{DC}}}. \quad (6)$$

As can be concluded from (6), the value of c_P is proportional to inverse values of $v_{s,max}/V_{dc}$ and $i_{s,max}/I_{dc}$. The value of c_P can be calculated for the typical class E PA, according to values of $v_{s,max}/V_{dc}$ and $i_{s,max}/I_{dc}$, which is 0.098.

VI. Simulation Results and Design Examples

The presented amplifier is simulated at 1 MHz, using ADS and PSpice software. An IRF530 MOSFET transistor is applied as a switch in the designed class E circuit. The first design example is simulated using ADS software. A switch model with relevant parasitic elements is used in the ADS simulation to model the switching device. The MOSFET on resistance ($R_{DS(on)}$ = 0.16 Ω) is considered, according to the IRF530 MOSFET datasheet. To validate the ADS simulation results, the second design example is simulated using PSpice software. The circuit values and design parameters of two design examples are the same, except the load resistance. The small difference in the load resistance is due to the MOSFET parasitic elements, which were considered in the PSpice simulation. Parasitic resistances and capacitances of the MOSFET are considered in the PSpice model. The IRF530 level 3 PSpice model is used in this paper. Simulated results of the first and second design examples are shown in Fig. 8 and Table 2. According to the PSpice simulation results, the normalized maximum MOSFET voltage and MOSFET current of the presented PA have been achieved 2.76 and 2.95, respectively. Subsequently, from equation (6), the c_P factor for the presented PA can be obtained as 0.122. The c_P factors of different amplifiers are compared in Table 3. According to the results, the presented HCN can improve both the c_P factor and the MOSFET voltage. More parameters of class E amplifier could be improved using a modified HCN, which we will address in future work. As mentioned, the drain impedance shapes the MOSFET voltage and currents of the amplifier. Therefore, several limitations of class E PA could be removed using a modified HCN.

TABLE I. Circuit Values of Designed Amplifier

V_{DC}	12 V
f_0	1 MHz
L	11 µH
C	2.53 nF
C_{sh}	5 nF
L_{N1}	7.8 µH
C_{N1}	360 pF
L_{N2}	10 µH
C_{N2}	10 pF

TABLE II. Design Examples Results

	First design example	Second design example
V_{in}	10 V	10 V
R	5.8 Ω	6.2 Ω
$v_{s,max}$	33.12 V	33.4 V
V_o	11.8 V	12.3 V

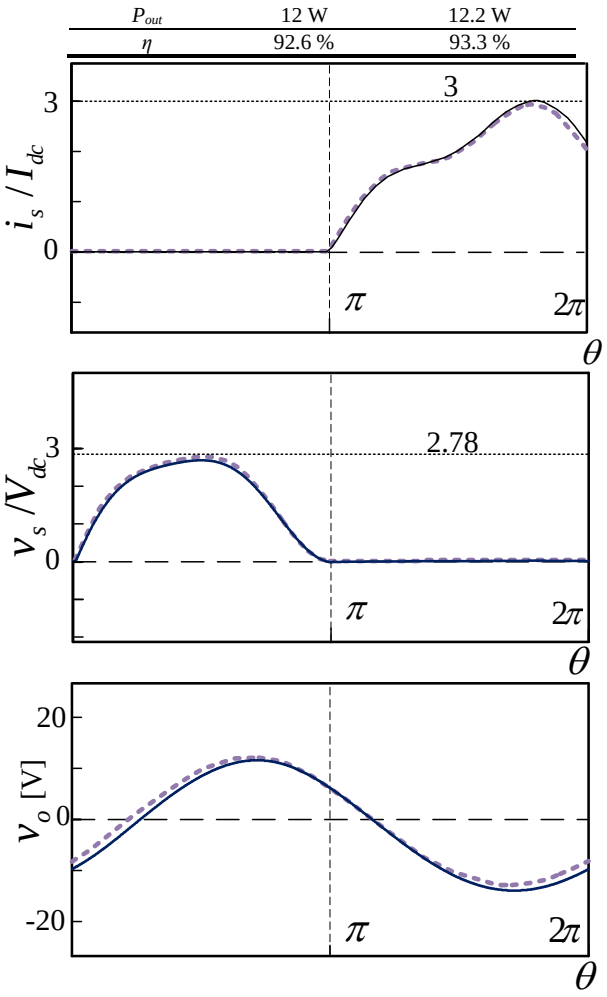

Fig. 8. Simulated waveforms of the presented amplifier using ADS (dashed line) and PSpice (solid line)

TABLE III. Output Power Capabilities (c_P) of Different Amplifiers

Amplifier Type	c_P
Class B	0.125
Class D	0.159
Class E	0.098
Class DE	0.079
This work	**0.122**

VII. Conclusion

A new harmonic control network (HCN) is inserted in typical class E power amplifier structure. According to the results, several parameters of class E PA are improved, using the applied HCN. The voltage stress of the presented amplifier is reduced, which relaxes the design limitations of the presented PA. Besides, the output power capability is increased, when compared with the other amplifiers. According to the results, the proposed amplifier structure presents both high-efficiency advantage of class E PA and high output power capability advantage of class D PA.

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