Differential Evolution based SHEPWM for Seven-Level Inverter with Non-Equal DC Sources

Fayçal CHABNI, Rachid TALEB, M'hamed HELAIMI
Electrical Engineering Department, Hassiba Benbouali University, Chlef, Algeria
Laboratoire Génie Electrique et Energies Renouvelables (LGEER)

***Abstract*—This paper presents the application of differential evolution algorithm to obtain optimal switching angles for a single-phase seven-level to improve *AC* voltage quality. The proposed inverter in this article is composed of two H-bridge cells with non-equal DC voltage sources in order to generate multiple voltage levels. Selective harmonic elimination pulse width modulation (SHPWM) strategy is used to improve the AC output voltage waveform generated by the proposed inverter. The differential evolution (DE) optimization algorithm is used to solve non-linear transcendental equations necessary for the (SHPWM). Computational results obtained from computer simulations presented a good agreement with the theoretical predictions. A laboratory prototype based on STM32F407 microcontroller was built in order to validate the simulation results. The experimental results show the effectiveness of the proposed modulation method.**

Keywords—selective harmonic elimination; multi-level inverters; differential evolution; cascade H-bridge inverters; optimization

I. INTRODUCTION

The direct current to alternative current (DC/AC) multi-level conversion systems have been drawing a lot of attention in the last few years especially for high voltage and renewable energy applications. The usage of power converters in high power applications have led to the development of various families and architectures such as Neutral Point Clamped (NPC)[1] Diode-clamped [2], and cascade multilevel inverters (CMLIs)[3].

The cascade multilevel inverters (CMLIs) have received a lot of attention due to their modular structure and simplicity of control; they offer a lot of advantages such as low switching losses [4], better electromagnetic compatibility [5] and low voltage stress on the switching devices [6]. The architecture can be formed by associating several individual H-bridge cells in series, and by adding more cells, the output voltage waveform become close to a sinusoidal waveform.

Several modulation strategies have been proposed and studied for the control of multilevel inverters such as Sinusoidal Pulse width modulation (SPWM)[7] and space vector pulse width modulation (SVPWM)[8]. A more efficient method called selective harmonic elimination pulse width modulation (SHE-PWM) is also used; the method offers a lot of advantages such as operating the inverters switching devices at a low frequency which extends the lifetime of the switching devices. The main disadvantage of this method is that a set of non-linear equations must be solved to obtain the optimal switching angles to apply this strategy.

Multiple computational methods have been used to calculate the optimal switching angles such as Newton-Raphson (N-R)[9], this method dependents on initial guess of the angle values in such a way that they are sufficiently close to the global minimum(desired solution). And if the chosen initial values are far from the global minimum, non-convergence can occur.

Selecting a good initial angle, especially for a large number of switching angles can be very difficult. Another approach is to use optimization algorithms such as genetic algorithm (GA) [10], firefly algorithm (FFA) [11] and particle swarm optimization (PSO)[12]. The main advantage of these methods is that they are free from the requirement of good initial guess.

The differential evolution (DE) is one of the most powerful optimization algorithms. Since its introduction in 1997 [13], the algorithm has drawn the attention of many scientists over the world, resulting in multiple variants derived from the original basic algorithm, with improved performance. The DE is a simple yet powerful algorithm; it is composed of three main operations mutation, crossover and selection [14]. The algorithm uses the difference of solution vectors to create new candidate solutions using the above-mentioned operators. This work investigates the use of (DE) as an optimization tool to implement the (SHEPWM) for a seven level inverter.

In [15] the author proposed the application of differential evolution for selective harmonic elimination in a three phase two level inverter with multiple switching angles in quarter of period to eliminate multiple low order harmonics, the main disadvantage of this work is that the proposed inverter cannot be used in high power application due to voltage stress exercised on the switching devices. This paper presents a simple and fast optimal solution of harmonic elimination of a seven level inverter with non-equal DC sources using the differential evolution algorithm. The algorithm is used to solve a system of non-linear equations that describes the waveform of the output voltage in order to obtain the optimal switching angles, to improve the output voltage quality.

This paper is organized as follows: the next section explains briefly the structure of the proposed multilevel inverter and its control, the third section covers the application of the differential evolution algorithm for the selective harmonic elimination, this section details the procedures to

obtain the optimal switching angles and the formulation of the objective function, the fourth section presents the simulation results obtained from the mathematical model of the system and the optimization method. The effectiveness of the selective harmonic elimination using DE is verified using a small scale laboratory seven level inverter based on STM32F407 Microcontroller unit, the section also presents and discusses the hardware implementation and the experimental results in details. The conclusion is presented in the last section.

II. TOPOLOGY

As mentioned before there are three main families of multilevel inverters. And those families are the diode clamped inverters, flying capacitor inverters and the cascade multilevel inverters. The multilevel cascaded configuration is a popular choice in high power applications, in addition to advantages mentioned before, this configuration does not require a large number of components and does not need clamping diodes or balancing capacitors [16-17], the modular structure of this topology allows easier maintenance.

Cascaded Multilevel Inverter topology rely on a simple principle based on the summation of voltages generated by each individual cell (H-bridge) to obtain a staircase output voltage waveform. Fig.2 illustrates the voltage waveform of a seven level inverter in a quarter of period. Fig.1 demonstrates the proposed single phase seven level asymmetrical inverter. It is formed by two H-bridges connected in series each bridge is powered by electrically isolated power supplies to generate the desired waveform.

Each H-bridge module is connected to its respective isolated DC source; each module can generate three voltage levels +V which is the positive voltage of the DC source ,0V and –V which is the negative voltage of the DC source , and as it can be observed in Fig.1 in order to obtain seven levels at the output of the inverter, the DC voltage source connected to the lower cell has to be twice the value of the DC source connected to the upper cell (Vdc2=2×Vdc1).

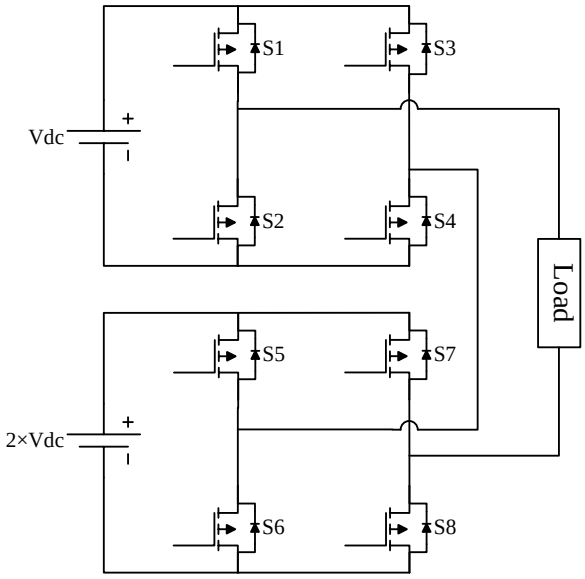

Fig. 1. Structure of the proposed multilevel inverter

The valid switching states for all possible combination of input voltage sources are given in Table.1. It can be seen that in order to generate a voltage level at least four switching devices have to be switched on.

TABLE I. SWITCHING STATES OF SEMICONDUCTOR DEVICES FOR 7-LEVEL INVERTER

	Switches state							
Voltage levels (P.U)	***S1***	***S2***	***S3***	***S4***	***S5***	***S6***	***S7***	***S8***
3	on	Off	off	on	on	Off	off	on
2	off	On	off	on	on	Off	off	on
1	on	Off	off	on	off	On	off	on
0	off	On	off	on	off	On	off	on
-1	off	On	on	off	off	On	off	on
-2	off	On	off	on	off	On	on	off
-3	off	On	on	off	off	On	on	off

III. SELECTIVE HARMONIC ELIMINATION USING DIFFERENTIAL EVOLUTION

The number of voltage levels that can be generated by CMLIs is generally presented by $2P+1$ where P represents the number of voltage levels or switching angles in a quarter waveform of the signal, and P-1 is the number of undesired harmonics that can be eliminated from the generated waveform. In a seven level inverter, the number of voltage levels in quarter waveform is three which means the number of harmonics that can be eliminated is two.

In order to eliminate the undesired harmonics, the switching angles θ_1, θ_2 and θ_3 represented in Fig.2 must be computed.

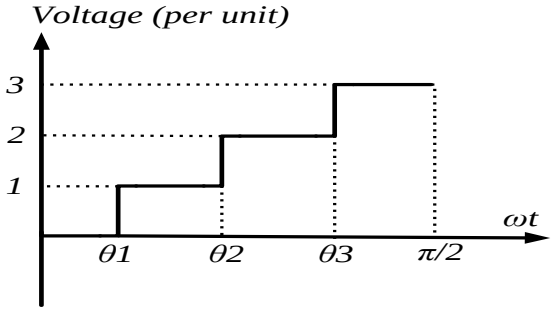

Fig. 2. quarter waveform of a seven-level inverter

For the staircase output voltage waveform of multilevel inverter as shown in Fig.2 there are 3 voltage levels (in quarter waveform) and 2 undesired harmonics.

To control the peak value of the output voltage to be V_1 and eliminate the 3rd and 5th harmonics the resulting equations and since the voltage waveform has quarter and half wave symmetry characteristics, the Fourier series expansion is given as:

$$V(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \left[\frac{4V_{dc}}{n\pi}\sum_{i=1}^{p}\cos(n\theta_i)\right]\sin(n\omega t) \qquad (1)$$

Where n is rank of harmonics, $n = 1,3,5, \dots$,and p =(N-1)/2 is the number of switching angles per quarter waveform., and θ_i is the i^{th} switching angle, and N is the number of voltage levels per half waveform. The optimal switching angles θ_1, θ_2

and θ_3 can be determined by solving the following system of non-linear equations:

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = M \\ H_3 = \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) = 0 \\ H_5 = \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \end{cases} \quad (2)$$

Where $M = (((N-1)/2)r/4)$, r is the modulation index.

The obtained solutions must satisfy the following constraint:

$$0 < \theta_1 < \cdots < \theta_p < \pi/2 \quad (3)$$

An objective function is necessary to perform the optimization operation, the function must be chosen in such way that allows the elimination of low order harmonics while maintaining the amplitude of the fundamental component at a desired value Therefore the objective function is defined as:

$$F(\theta_1\theta_2 \ldots \theta_p) = \left(\sum_{n=1}^{p} \cos(\theta_n) - M\right)^2 + \left(\sum_{n=1}^{p} cos\,(3\theta_n)\right)^2 + \left(\sum_{n=1}^{p} cos\,(5\theta_n)\right)^2 \quad (4)$$

The optimal switching angles are obtained by minimizing Eq (4) subject to the constraint Eq(3).The main problem is the non-linearity of the transcendental set of Eq(2), the differential algorithm is used to overcome this problem.

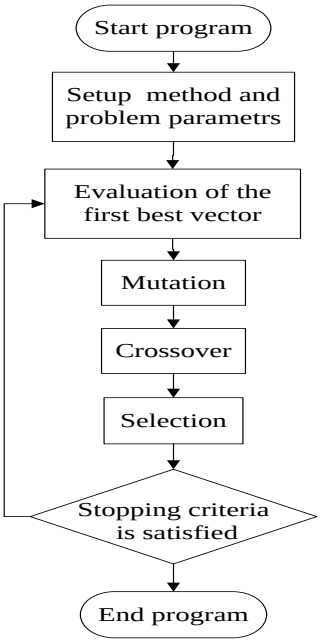

Fig. 3. Flowchart of DE algorithm

The differential evolution algorithm (DE) is an optimization method is composed of three main steps initialization, mutation and crossover. The general structure of a DE program is shown in Fig.3. The algorithm perturbs the population of vectors by employing the mutation, whereas its diversity is controlled by the cross-over process [18].

In the case of SHPWM, differential evolution algorithm is used as an optimization tool to perform a random search for the global minima, which is forcing the objective function (4) towards an allowable error value.

The optimization process starts by initializing the necessary parameters of the algorithm, such as the population size (*NP*), crossover probability (*CP*), upper and lower bounds (θ_{min} and θ_{max}) and the maximum number of iterations. It should be noted that the boundaries must satisfy equation (3). The next step is to randomly generate an initial population of switching angles in this process the algorithm creates

$$\theta_{ij}^{(0)} = \theta_{\min ij} + rand_i(\theta_{maxj} - \theta_{minj}) \quad (5)$$

With *i*=1,2,…,*NP* and *j*=1,2,…,*N*

Where $\theta_{ij}^{(0)}$ is the initial population, *i* presents the population size in this study *NP*=50, *j* is the number of decision variables which represents the number of switching angles, in case of a seven level inverter *N*=3. After the initialization process, the generated population is evaluated, the evaluation of the fitness of each individual is carried out by using (4).

The mutation process creates a mutant v_{ij} vector based on the initial population; this process is described by the following expression

$$v_{ij} = X_{r1} + F(X_{r2} - X_{r3}) \quad (6)$$

Xr1, *Xr2* and *Xr3* are vectors randomly sampled from the generated population, $X_r = [\theta_{i1}, \theta_{i2}, \ldots, \theta_{iN}]$, the indices *r1*, *r2* and *r3* are integers randomly chosen from the range [1 *NP*], they are also chosen to be different from the index *i*, the parameter *F* is the mutation constant which controls the amplification of the differential variation $(X_{r2} - X_{r3})$, the value of this parameter is randomly generated from the range [0 1], it should be noted that multiple mutation methods were reported in[19].

To improve the diversity of the population, the crossover operation comes into play, after generating the mutant vector v_{ij}through mutation, this operation assures the production of fitter individuals, the result of this process is a vector u obtained by mixing the components of $v_{ij}$and Xi the process can be expressed as:

$$u = \begin{cases} v_{ij}\ if\ rand \le CP\ or\ j = j_{rand} \\ Xi \qquad\qquad otherwise \end{cases} \quad (7)$$

Where *rand* is a random number in the range of [0 1], *CP* is the crossover probability constant, it controls the diversity of the population and it has a value between 0 and 1 [20], j_{rand} is randomly chosen index. Once the crossover process is completed, the selection process comes into play to decide whether the u_i or X_i vector survives for the next generation, this process is carried out to choose the fittest individual. The selection process can be expressed mathematically as:

$$X_i^{G+1} = \begin{cases} u_i^{G+1}\ if\ f(u_i^{G+1}) < f(X_i^G) \\ X_i^G \qquad\qquad otherwise \end{cases} \quad (8)$$

Where $f(X)$ is the objective function to be minimized, and G is the generation count. Once the selection operation is completed, the algorithm loop is repeated until the stopping criteria is satisfied, in this study the DE algorithm is limited by maximum number of iterations $Nitr$=1000 .

IV. Simulation Results

In order to prove the theoretical predictions and to test the effectiveness of the proposed algorithm, the control method and the proposed inverter were developed and simulated using MATLAB/SIMULINK scientific programming environment; the optimization program was executed on a computer with Intel(R) Core(TM) i3 CPU@ 2.13GHz Processor and 4GB of RAM, the optimization algorithm takes 1274.463 seconds to complete the computation process.

To verify the effectiveness of the proposed method, total harmonic distortion (*THD*) is used as a performance indicator to evaluate the quality of output AC voltage waveform generated from the multilevel inverter, the THD is defined as the total amount of harmonics related to the fundamental, it can be calculated using the following formula:

$$THD\% = \frac{\sqrt{\sum_{n=3}^{19} {H_n}^2}}{H_1} \times 100 \qquad (9)$$

The differential evolution algorithm is used to find the switching angles for each value of modulation index r; the total harmonic distortion is computed also for each r, Fig.4 illustrates optimal switching angles (in degrees) versus modulation index r with $r \in [0.2\ 0.95]$, the angles are computed with a fine step-size of 0.01, and it can be seen that in some ranges of the modulation index, the obtained solutions exceeded the 90 degrees limit, those solutions are not going to be taken in consideration . Fig.5 shows the variation of the total harmonic distortion versus the modulation index, these results are obtained by using equation (9) and (2).

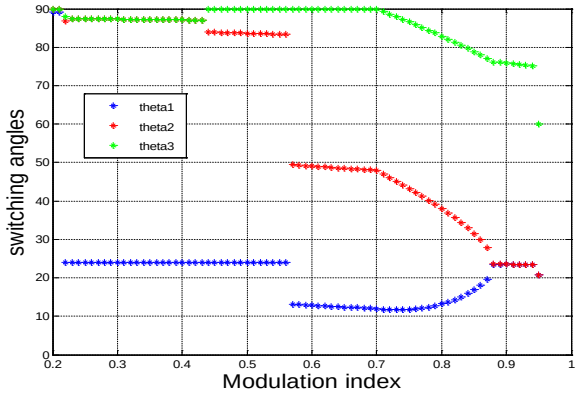

Fig. 4. Switching angles versus modulation index

To confirm the validity of the proposed algorithm, angles extracted from the obtained switching angles were applied to a mathematical model of a seven-level inverter. The fundamental frequency used in this simulation is 50Hz, the input voltages of the first bridge (upper cell) and the second bridge (lower cell) are respectively V_{dc1}=25V, Vdc2=50V the switching angles to be applied (in degrees) are: θ_1= 16.87°, θ_2= 31.57° and θ_3= 78.82° which correspond to the modulation index r= 0.85.

Fig.6 and Fig.7 show the voltage waveforms generated respectively by the upper and the lower cell. From those two figures it can be seen that each bridge is responsible of generating three voltage levels. The summation of two voltages will generate the desired seven-level staircase waveform.

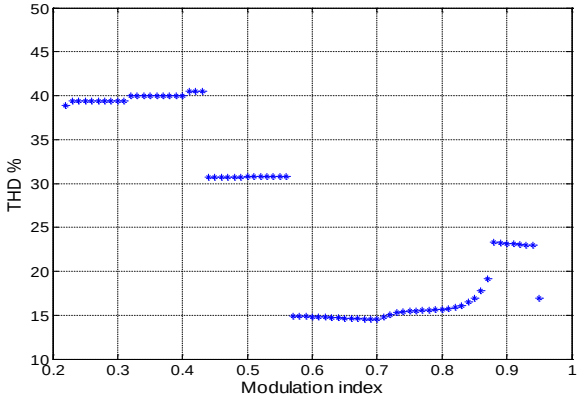

Fig. 5. THD versus modulation index

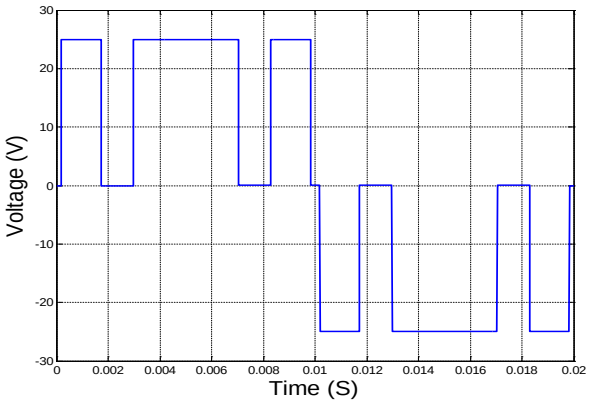

Fig. 6. Output voltage of the upper cell

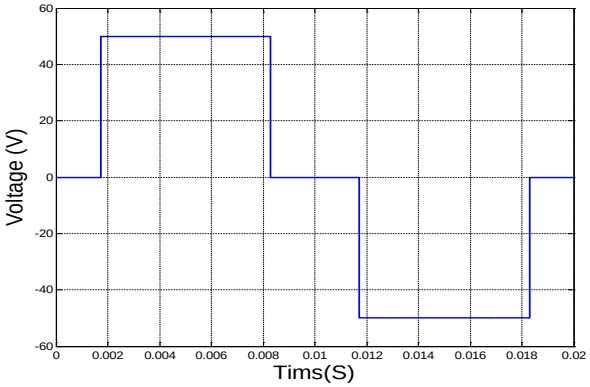

Fig. 7. Output voltage of the lower cell

Fig.8 shows the output voltage obtained from the multilevel inverter for r=0.85 .Fig.9 shows its spectra of the output voltage. As expected, the selected harmonics (3rd and 5th) are successfully eliminated, the total harmonic distortion *THD*=16.97%. Fig.10 demonstrates the gating signals for the semiconductor switches from S1 to S8.

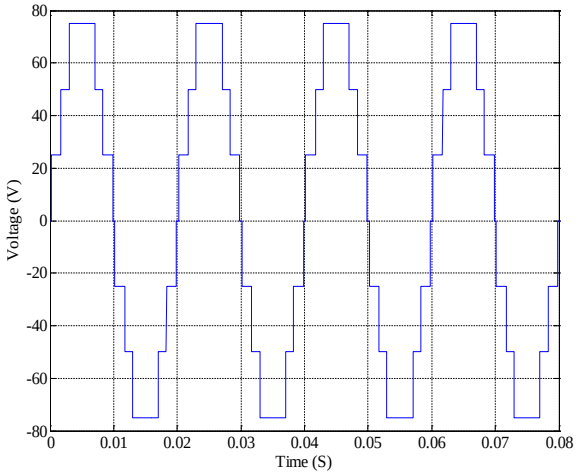

Fig. 8. Output voltage generated by the inverter

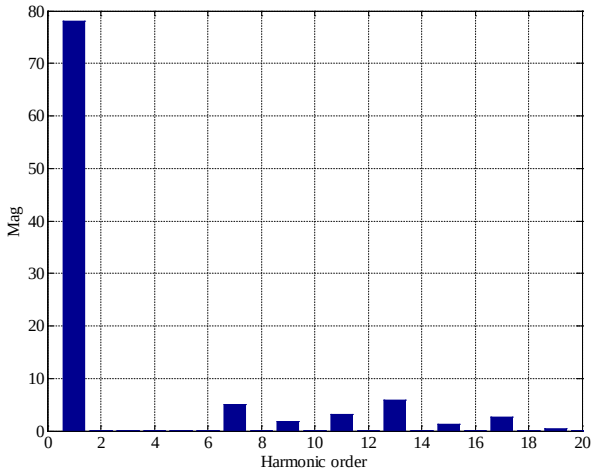

Fig. 9. FFT of 7-level inverter voltage output

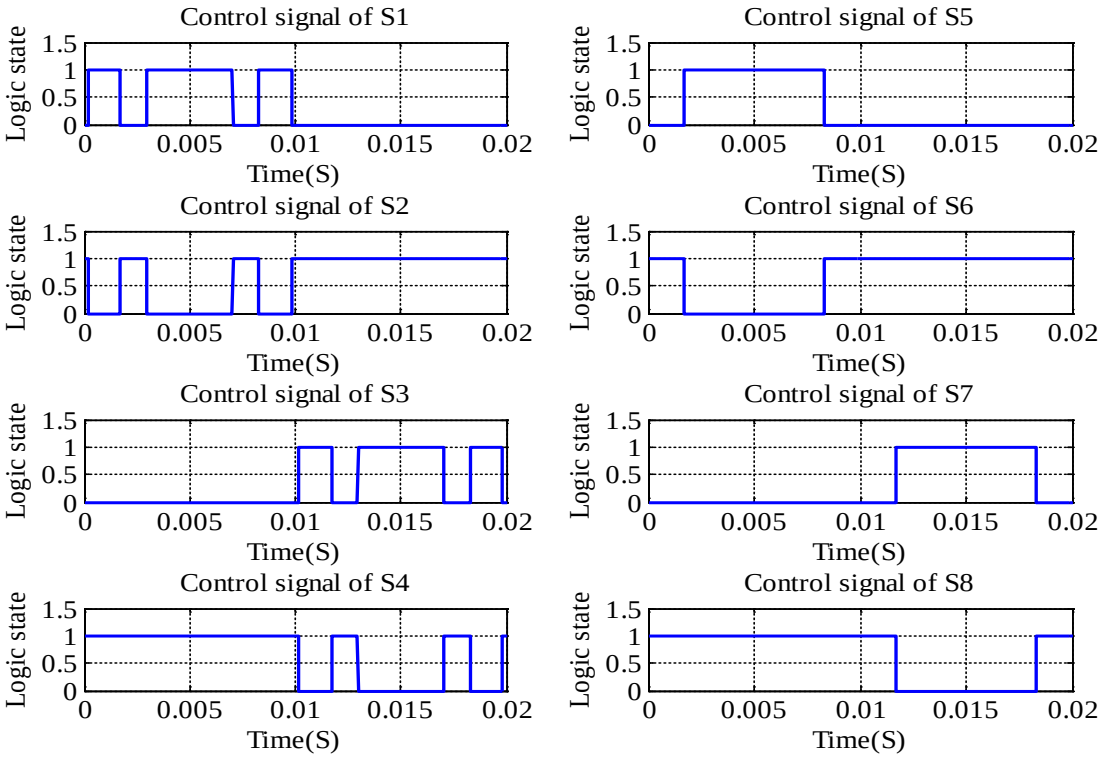

Fig. 10. Fig. Gating signals

V. Experimental Results

The proposed method was validated by building a small scale laboratory prototype, IRF640(200V,18A) MOSFETs were used as switching devices SDS1000 oscilloscope100MHz 500Ms/s was used to capture the voltage waveforms, an STM32F407 microcontroller was used to generate control signals for the switching devices, the FFT analysis was performed by computer connected to the oscilloscope trough USB.

Fig.11 presents the block diagram of the laboratory prototype of the seven level inverter that is implemented as mentioned before with eight IRF 640 Metal Oxide Semiconductor Field Effect Transistors (MOSFET), it should be noted that those switching devices are also equipped with freewheeling diodes. TLP250 photocouplers are used to provide electrical isolation between the MCU and the power circuits, and also to provide proper and conditioned gate signals to the MOSFETs. The switching angles are calculated using differential evolution algorithm by a computer, once the switching angles are obtained, the switching patterns for each switching device will be stored inside the memory of the MCU as a look-up table.

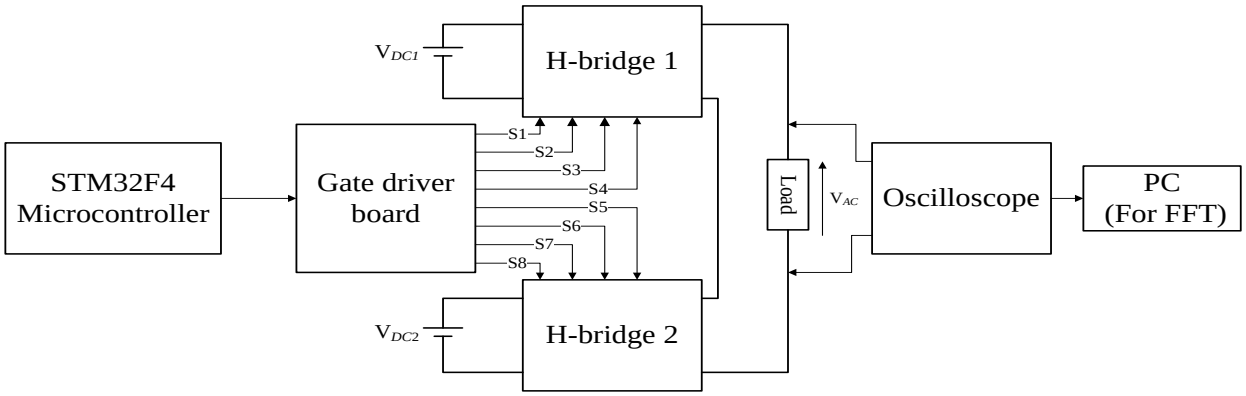

Fig. 11. Block diagram of the hardware setup

The single phase seven level voltage pattern obtained in simulation shown in Fig.8 is experimentally validated and the result is shown in Fig.14 the voltage waveforms generated by the upper and lower cell obtained in simulation presented in Fig.6 and Fig.7 respectively , are also experimentally validated, the results are presented in Fig.12 and Fig.13.

Fig.19 illustrates the FFT analysis of the experimentally obtained voltage waveform; it can be clearly seen that the 3rd and the 5th harmonics were successfully eliminated. This result matches perfectly the simulation result presented in Fig.9. The total harmonic distortion of the experimental voltage waveform is 15.85% which is very close to the simulation result.

Fig.15, Fig.16 Fig.17and Fig.18 illustrates the gating signals generated by the STM32F407 microcontroller unit (MCU) for the switching devices; these figures validate the simulation results presented in Fig.10.

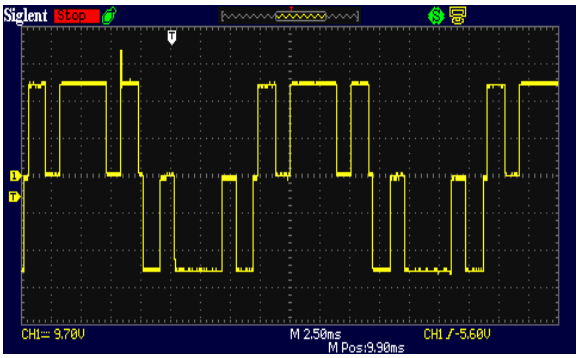

Fig. 12. Output voltage waveform generated by the upper cell

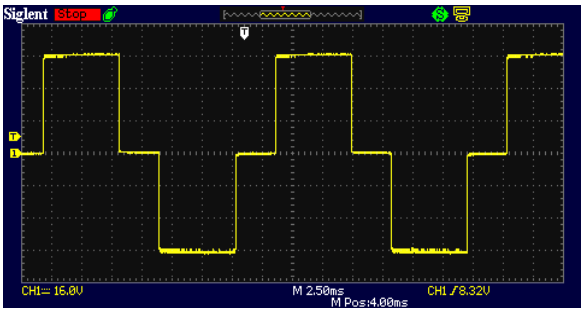

Fig. 13. Output voltage waveform generated by the upper cell

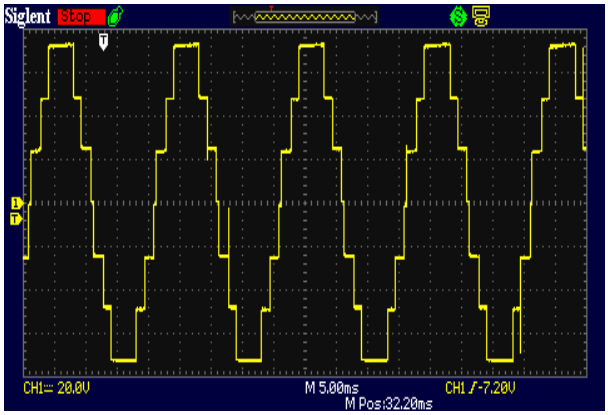

Fig. 14. Output voltage waveform generated the proposed multilevel inverter

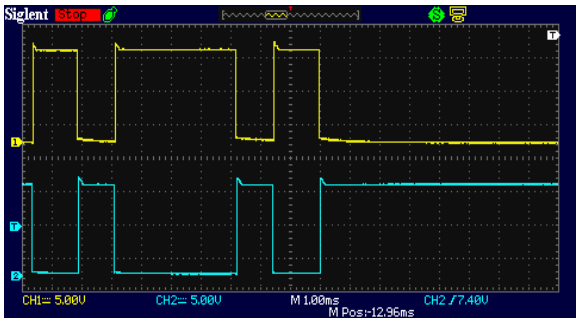

Fig. 15. Control signals generated by the MCU for S1 (yellow trace) and S2 (Blue trace)

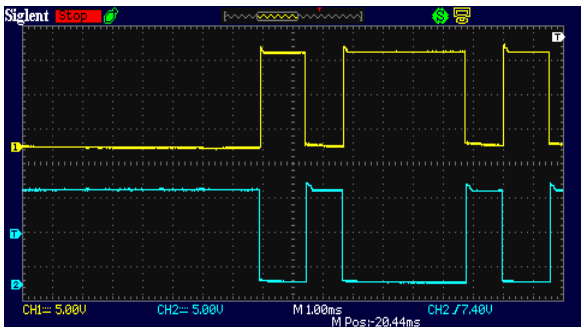

Fig. 16. Control signals generated by the MCU for S3 (yellow trace) and S4 (Blue trace)

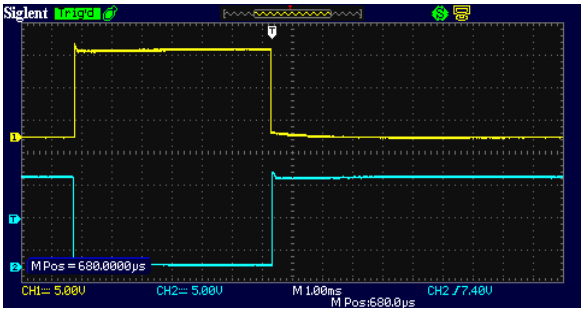

Fig. 17. Control signals generated by the MCU for S5 (yellow trace) and S6 (Blue trace)

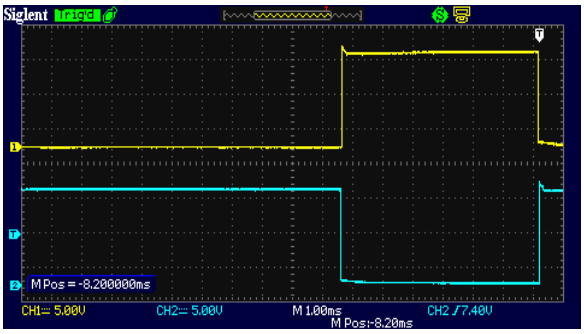

Fig. 18. Control signals generated by the MCU for S7 (yellow trace) and S8 (Blue trace)

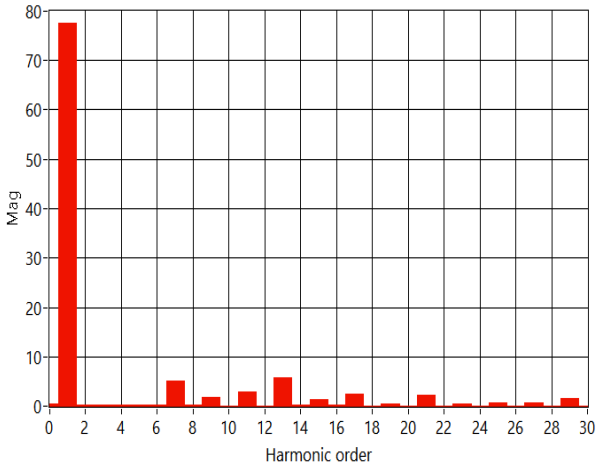

Fig. 19. FFT of 7-level inverter experimental voltage output

VI. Conclusion

This paper illustrates the use of differential evolution algorithm in selective harmonic elimination for a single phase seven level voltage source inverter to improve the harmonic quality of the generated output voltage. The proposed multi-level inverter with non-equal DC sources has the advantage of generating multiple voltage levels with less switching components. The differential evolution algorithm is used to solve a set of non-linear equations in order to obtain the optimal switching angles to perform the (SHE) modulation strategy. Optimal switching angles are investigated over the range $r \in [0.2\ 0.95]$. The total harmonic distortion (THD) was chosen as a performance indicator in order to examine the effectiveness of the proposed algorithm. The validity of the method has been proven by computer simulation using Matlab/Simulink scientific programming environment and verified by experimental hardware set-up based on STM32F407 microcontroller. The obtained results from the simulation and hardware show a good agreement with the theoretical prediction.

References

[1] H. Wang, Y. F. Liu and P. C. Sen, "A neutral point clamped multilevel topology flow graph and space NPC multilevel topology," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 3615-3621.

[2] G. P. Adam, S. J. Finney, O. Ojo and B. W. Williams, "Quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation," in IET Power Electronics, vol. 5, no. 5, pp. 542-551, May 2012.

[3] Z. Chunyan and L. Zhao, "Advanced compensation mode for cascade multilevel static synchronous compensator under unbalanced voltage," in IET Power Electronics, vol. 8, no. 4, pp. 610-617, 4 2015.

[4] A. Edpuganti and A. K. Rathore, "Optimal Low Switching Frequency Pulsewidth Modulation of Nine-Level Cascade Inverter," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 482-495, Jan. 2015.

[5] M. Hajizadeh and S. H. Fathi, "Selective harmonic elimination strategy for cascaded H-bridge five-level inverter with arbitrary power sharing among the cells," in IET Power Electronics, vol. 9, no. 1, pp. 95-101, 1 20 2016.

[6] C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," in IET Power Electronics, vol. 6, no. 3, pp. 468-477, March 2013.

[7] B. Karami, R. Barzegarkhoo, A. Abrishamifar and M. Samizadeh, "A switched-capacitor multilevel inverter for high AC power systems with reduced ripple loss using SPWM technique," Power Electronics, Drives Systems & Technologies Conference (PEDSTC), 2015 6th, Tehran, 2015, pp. 627-632.

[8] K. C. Jana and S. K. Biswas, "Generalised switching scheme for a space vector pulse-width modulation-based N-level inverter with reduced switching frequency and harmonics," in IET Power Electronics, vol. 8, no. 12, pp. 2377-2385, 12 2015.

[9] T. Mistry, S. K. Bhatta, A. K. Senapati and A. Agarwal, "Performance improvement of induction motor by Selective Harmonic Elimination (SHE) using Newton Raphson (N-R) method," 2015 International Conference on Energy Systems and Applications, Pune, India, 2015, pp. 364-369.

[10] Erkan Deniz, Omur Aydogmus, Zafer Aydogmus, Implementation of ANN-based Selective Harmonic Elimination PWM using Hybrid Genetic Algorithm-based optimization, Measurement, Volume 85, May 2016, Pages 32-42

[11] M. Gnana Sundari, M. Rajaram, Sujatha Balaraman, Application of improved firefly algorithm for programmed PWM in multilevel inverter with adjustable DC sources, Applied Soft Computing, Volume 41, April 2016, Pages 169-179

[12] Shimi Sudha Letha, Tilak Thakur, Jagdish Kumar, Harmonic elimination of a photo-voltaic based cascaded H-bridge multilevel inverter using PSO (particle swarm optimization) for induction motor drive, Energy, Volume 107, 15 July 2016, Pages 335-346,

[13] S. Das and P. N. Suganthan, "Differential Evolution: A Survey of the State-of-the-Art," in IEEE Transactions on Evolutionary Computation, vol. 15, no. 1, pp. 4-31, Feb. 2011.

[14] Z. Salam, A. M. Amjad and A. Majed, "Using Differential Evolution to Solve the Harmonic Elimination Pulse Width Modulation for Five Level Cascaded Multilevel Voltage Source Inverter," Artificial Intelligence, Modelling and Simulation (AIMS), 2013 1st International Conference on, Kota Kinabalu, 2013, pp. 43-48.

[15] A.Hiendro, "Multiple switching patterns for SHEPWM inverters using Differential evolution algorithms" in International Journal of Power Electronics and Drive Systems, vol.1, no2, pp94-103,Dec 2011

[16] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu and S. Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review," in IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 135-151, Jan. 2016.

[17] J. Han, T. Yang, D. Peng, T. Wang and G. Yao, "Model predictive control for asymmetrical cascaded H-Bridge multilevel grid-connected inverter with flying capacitor," IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, 2014, pp. 1611-1616

[18] R. Vijayakumar, C. Devalalitha, A. Nachiappan and R. Mazhuvendhi, "Selective harmonic elimination PWM method using two level inverter by differential evolution optimization technique," Science Engineering and Management Research (ICSEMR), 2014 International Conference on, Chennai, 2014, pp. 1-6.

[19] M. I. Mohd Rashid, A. Hiendro and M. Anwari, "Optimal HE-PWM inverter switching patterns using differential evolution algorithm," Power and Energy (PECon), 2012 IEEE International Conference on, Kota Kinabalu, 2012, pp. 32-37.

[20] C. Sun, H. Zhou and L. Chen, "Improved differential evolution algorithms," Computer Science and Automation Engineering (CSAE), 2012 IEEE International Conference on, Zhangjiajie, 2012, pp. 142-145.