# Modeling and FPGA Implementation of a Thermal Peak Detection Unit for Complex System Design

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Abstract—This paper, presents the modelization and the implementation of a thermal peak detection unit for complex system design. The modelization step starts with modeling the formula of the heat source using Simulink/Matlab tool, is the main objective of this work. Then the input temperature, the angles, the distance as well as certain frequencies, will be obtained from this formula using the GDS (gradient Direction Sensor) method based on RO (Ring Oscillator). Before the transition to the implementation in FPGA board, the use of VHDL code is necessary to describe the thermal peak detection unit, in order to verify and validate the whole module. This work offers a solution to thermally induced stress and local overheating of complex systems design which has been a major concern for the designers during the design of integrated circuit. In this paper a DE1 FPGA board cyclone V family 5CSEMA5F31C6 is used for the implementation.

### Keywords—Thermal peak; complex system design; MATLAB; GDS; RO; FPGA; DE1

### I. INTRODUCTION

Integrating complex systems on a single System on Chip (SoC) has become possible with the evolution of technology. The high integration in the SoC systems increase the power density of power consumed and dissipated, which increase the internal temperature of the chip. The more the chip shrinks, the more it is overheated. It is known that high temperatures as well as thermal variations reduce the life and reliability of semiconductor layers of complex systems. In theory current technologies limit the maximum temperature to 125 degrees Celsius, but practically checking this restriction is not an easy task. The designer must take into account many aspects such as maximum voltages, the effect of heat sinks and ventilators. There has been recently huge interest by several research studies on the detection and management of thermal peaks [1]-[5]. This research is similar in general purpose but differs greatly in the techniques used and the methodology applied, it all depends on the conditions considered in the study and the nature of the electronic system. A good study was done in [6] and a new technique was introduced. This paper models and implements in a FPGA board a thermal peak detection unit for circuits of high-complexity and high-density. On complex systems, the heat is accumulated from one cycle to another throughout their operation [7] which requires a deep study at the junction level. As a result the high temperatures as well as the variation of the thermal gradient reduce the lifetime and the reliability of semiconductor thin films. Regardless of the type of FPGA card used, the maximum temperature allowed by current technologies is 125°C like mentioned earlier [8]. In order to meet this requirement, the designer must deal with several aspects at the same time, such as total dissipated power, heat dissipation effect, cooling mode, PCB position, ambient temperature and the influence of the equipment used in proximity.

The GDS (gradient Direction Sensor) method [9]-[10] presents a good and easy solution to localize the thermal peak, in the simplest case it consists of three well positioned sensors that convert signals from electrical signal to frequencies in order to locate the thermal peak. Despite the use of the GDS method, the originality of this work rests on the modeling and implementation of a network of thermal sensors each one is actually a ring oscillator (RO) composed of six inverters to characterize the thermo mechanical stress of a complex system, Ring Oscillator (RO) and the GDS are explained in detail in [11] and [12]. Our methodology consists on the Development of a VHDL code to model the thermal peak localization equation under Matlab tool, using the GDS (gradient Direction Sensor) technique explained before, from each cell composed of three sensors we can obtain information on the temperature distribution and partly on the position of the heat source. This help to predict the thermal peak and to evaluate the thermo mechanical stress associated [13]. This means that, with the aid of a sensor network, it's easy to know the temperature values in some places in the structure, but this operation can only be possible after the conversion of the electrical signal to the frequency values, which is obtained after calculation, gives information on the thermal gradient direction. Based on this information the prediction of the temperature value associated with the heat source and the thermo mechanical stress distribution in the entire IC structure can be feasible. This approach is used as a methodology to model and implement the thermal peak detection equation to predict the temperature of a single heat source Ts on the surface of a given complex system. In Section 2, the development of the thermal peak localization model is discussed. Section 3 describes the implementation of VHDL code of the thermal peak detection unit on the FPGA board to verify and validate the results obtained.

#### II. THE MODELIZATION OF THE THERMAL PEAK LOCALIZATION UNIT

### A. Description of the GDS method adopted

The GDS method is in general a technique for evaluating a single heat source on the chip surface. This method has been studied and analyzed for its applicability as inverse engineering problem which is capable of detecting the thermal peaks and associated thermo-mechanical stress on the critical surface areas of large VLSI devices. In order to obtain information about heat source parameters, one only needs to know from where the phenomenon is distributed and sometimes how fast it is changing. The geometrical coordinates and an estimation of the investigated heat source can be obtained by applying the GDS method [1], [5]. In order to calculate the temperature of the heat source, the thermal peak detection module designed makes it possible to obtain this information by having at its input the angles, the distance h as well as certain frequencies. Although this module is optional, it is VHDL coded in order to have a thermal peak detection unit offering a plurality of services. The formula of the heat of this module is:

$$\frac{\frac{H}{a}(fc_1 - fa_1)(\sqrt{3} + \tan\alpha_2)(1 + \tan^2\alpha_1)}{\sqrt{3}(1 - \tan\alpha_1\tan\alpha_2) - (\tan\alpha_1 + \tan\alpha_2)} + fa_1 \leftrightarrow Ts \quad (1)$$

Equation (1) of localization of the thermal peak, takes in consideration the angles  $\alpha 1$  and  $\alpha 2$ , and the frequency fc1 and fa1 represents the description of a single heat source Ts with the GDS method. In order to obtain the temperature value of a single punctual heat source, the distance between the sensor and this source should be calculated. Two sensor cells are required for this purpose (Fig. 1). The cells are placed at a given distance H and each of them gives information about angle  $\alpha 1$  and  $\alpha 2$  in direction of the heat source. Under the consideration that "a" is relatively small, we can assume that the heat source and the center of the cells from a triangle in which the length of one side and values of the angles adjacent to this side are known, like illustrated in the following Fig. 1.



Fig. 1. The principle of detection by GDS of a source of heat based on three sensors RO.

This module based on the GDS method will be designed and tested afterwards using VHDL code.

### *B. The modelization of the thermal peak localization unit using Simulink*

The following Fig. 2 to 7 shows the representation and modeling of (1) in order to detect and localize the thermal peak by Simulink <sup>TM</sup> blocks.



Fig. 2. Calculation system with Matlab/Simulink.







Fig. 4. The Simulink blocks of the first module.





Fig. 5. The Simulink block subsystem of the second computing module.





Fig. 7. Structure of the thermal peak detection module under Matlab / simulink

Fig. 7 shows the modeling of all the Matlab/Simulink blocks in which the estimation and localization of the temperature of the heat source Ts is calculated.

## C. Tests and results of the thermal peak module using the display option

To test the realized thermal peak localization module under Matlab/Simulink of the heat source Ts introduced before in (1), the relation between the temperature and the frequency given in Fig. 8 is used, this study is found in [12] for T=25 °C, f=1 MHz. As an example it can be assumed that  $fa_1 = fc_1 = 1$  MHz this new values should be replaced with those in (1) with this new value we will get Ts=1°C at the end. To validate the module the same thing is done the frequencies  $fc_1$  and  $fa_1$  are replaced with the value 1 MHz and we get Ts=1.016 °C like shown in the display of Fig. 2. The answer corresponds to that obtained in (1). The flowing Table 1 explains this.



Fig. 8. Normalized ring-oscillator frequency response versus temperature.

The Fig. 8 shows the thermal evolution as a function of the frequency of the ring oscillator. For example, at 25 °C f=1 MHz, this information is used to test and validate our modelization in comparison with the heat equation as mentioned in the following table:

TABLE I. Test Table of Our Modelization in Comparison with the Equation of A Single Heat Source at 25  $^\circ\mathrm{C}$ 

Test case	Ts (°C) from equation (1)	Ts (°C) from modelization
$fa_1 = fc_1 = 1 MHz$	1	1.016

According to this table practically the same value is shown in option display, see Fig. 2 theoretically found by the equation (1), this validates the thermal peak detection unit module in a complex system based on (1) using Simulink of Matlab.

## D. Tests and results of the thermal peak module using the scope option

This section shows how much information can be found on the location of the thermal peak at the same frequency and the same temperature of the ring oscillators knowing that this type of sensor can only determine the necessary information if it receives sinusoidal signals, therefore a sinusoidal signal as an input of our module should be defined in this case, Fig. 9 shows the results found.



Fig. 9. Simulation of the thermal peak detection module shown by scope.

The simulation shown in Fig. 9 also confirms the correct functioning of the calculation module, as mentioned before in the results displayed by the scope option, within a timeframe of 308 ms, the module receives five information in order to characterize the thermal peak, this result validates the techniques and the methodology adopted to model (1). These found results will be used after in the implementation in the FPGA card to confirm and validate the good operation of the module.

### III. EXPERIMENTAL IMPLEMENTATION AND RESULTS

The main purpose of this section is the implementation and validation of the modelization results and simulation by Matlab /Simulink. VHDL code is used to describe the module to facilitate the development of its architecture for its implementation in complex system design. This architecture is modeled in high-level language, and simulated to assess its performance and finally implemented on FPGA. The simulation results are validated by using the software Modelsim under Quartus Prime, which allows simulating the behavior of the system in time. Our design flow will be divided parts: simulation, synthesis, main into three and implementation of the VHDL code on FPGA. A description of each part will be presented in the next paragraphs.

### A. Creation and simulation of the VHDL code

This part, presents the description of the thermal peak detection unit using a VHDL code editor. The code editor used is Modelsim. Fig. 10 shows the top-level module of our module.



Fig. 10. Top level of the thermal peak detection module.

After generating the two .vhd files (the primary file system and the "Test Bench" file) with the "System Generator" the role of the Quartus Prime Navigator comes in order to synthesize the design and generate the RTL files as shown in Fig. 11.



Fig. 11. Structure of the thermal peak detection module in Quartus Prime tool.

The structure of the thermal peak detection module after synthesis with Quartus Prime from Altera is shown in Fig. 11. The VHDL code implemented was validated based on the modelization designed before. In this part the simulation will be run with the same conditions used in Tab. I, to validate the experimental results. Fig. 12 shows the results found by the simulation using the Modelsim tool.



Fig. 12. Display results of simulation the VHDL code.

The value circled in red in Fig. 12, validates the VHDL code since it is the same value of Ts found before as shown in the comparison between our modelization and (1) shown in Fig. 2 and Table 1. This means that the VHDL code is correct and the modelization step is designed correctly. In this paper, an equation of single heat source based on GDS (gradient Direction Sensor) method for thermal peak detection is modeled, simulated and verified with a VHDL code and a 'test bench' at the laboratory LIMA the results found meet the initial specifications.

## *B.* Implementation and downloading of the VHDL code on DE1

Once compiled after the assignment of the pins, the program is ready to be downloaded on the card DE1 cyclone V a family and 5CSEMA5F31C6 as a device. Fig. 13 shows that the VHDL code is downloaded successfully on the card.

ISP to allow background p	l programming when a	vailable								
File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAM
<none></none>	SOCVHPS	00000000	<none></none>							
output_nes/sim.sor	DCSEMADES1	UUAF6DAD	UUAF6DA6	v						
		IASF31								

Fig. 13. Downloading the code of DE1 Altera cyclone V.



Fig. 14. The value shown on the LCD after the implementation of DE1 Altera cyclone V.

After the download, the program was running and then the outputs were shown. The clock is at 50 MHz, so the outputs should change with a frequency of 50 MHz and the following Fig. 14 shows the value  $(1^{\circ}C)$  at 15 second after implementation on LCD reader without floating point.

Fig. 14 shows that the value displayed on the LCD matches the results found before. The simulation and implementation on DE1 FPGA board can be applied in any kind of environment to get improved performance with respect to the conventional schematic; it is also able to keep the temperature constant at the desired value regardless of changes in the load or environment. Thus, the overshooting problem can be solved up to great extent. One of the important issues in the field of electronics is overheating problems especially when it comes to integrated and complex systems and microsystems, but the mean question is how to perform thermal monitoring, to indicate overheating situations, without control. The traditional approach consists of many sensors all over the chip, and then their output can be shown simultaneously and be compared to the reference voltage recognized as the level of overheating. The idea of the proposed method is to predict the local temperature and gradient along the given distance in some places only on the monitored surface and evaluates obtained several real-time information in a short area in order to predict the temperature of the heat source. Therefore, in the case of a SoC device, there is no place on the layout for complicated unit to perform calculations such as described in paper [10], but there is also no need, because we only want to detect overheating situations. These peaks are essential when monitoring the thermal matrix to avoid a critical induced thermo-mechanical stress. In addition, in most cases, overheating occurs in only one location.

### IV. CONCLUSION

In this paper, a new method to evaluate and predict thermal peak of complex system design, based on the GDS method. In this work a thermal peak detection unit was designed using the heat equation of a single heat source. The modelization of this unit was designed by simulink/Matlab, and was described with a VHDL coder, after the simulation, the unit was implemented on the DE1 FPGA board. Thus, the factors of the heat equation requiring special attention during the development of a thermal peak detection unit, we can mention the number of sensors, their proximity, their spatial distribution and their network interconnections. The application of this method will be the basis for future developments of the detection algorithm for several sources of heat. These architectures were modeled in high-level language, simulated to evaluate their performance and implemented on FPGA. The implementation of more complex design systems, the purpose of the applications that will be integrated using this work is to get more information in real-time, this will help the designers to react at the right time, also the proposed module, bringing other benefits such as support to characterize and locate each thermal peak. This will show other types of information, and communication methods on thermal peak in a reliable way and integrate them without any analog device.

#### REFERENCES

- Bougataya, M, Lakhsasi, A, & Massicotte, D, "VLSI thermo-mechanical stress analysis by gradient direction sensor method", In Electrical and Computer Engineering, IEEE Canadian Conference, pp. 710-713, (May. 2015).
- [2] Janicki, M, Zubert, M, & Napieralski, A, "Application of inverse problem algorithms for integrated circuit temperature estimation", Microelectronics journal, pp. 1099-1107, (1999).
- [3] Lopez-Buedo, S, & Boemo, E, "Making visible the thermal behaviour of embedded microprocessors on FPGAs: a progress report", In Proceedings of the ACM/SIGDA 12th international symposium on Field programmable gate arrays, pp. 79-86, (2005).
- [4] Velusamy, S, Huang, W, Lach, J, Stan, M, & Skadron, K, "Monitoring temperature in FPGA based SoCs, In Computer Design: VLSI in Computers and Processors, Proceedings, IEEE International Conference, pp. 634-637, (Oct. 2005).
- [5] Wójciak, W., & Napieralski, A, "Thermal monitoring of a single heat source in semiconductor devices the first approach", Microelectronics journal, pp. 313-316, (1997).
- [6] V. d'Alessandro, M. De Magistris, A. Magnani, N. Rinaldi, S. Grivet-Talocia, & S. Russo, "Time domain dynamic electrothermal macromodeling for thermally aware integrated system design", In Signal and Power Integrity (SPI), 17th IEEE Workshop, pp. 1-4, (May. 2013).
- [7] Jaeger, R. C, Suhling, J. C, Carey, M. T, & Johnson, R. W, "A piezoresistive sensor chip for measurement of stress in electronic packaging", In Electronic Components and Technology Conference IEEE, Proceedings, pp. 686-692, (June. 1993).
- [8] Oukaira, A, Lakhssassi, A, Fontaine, R, & Lecomte, R, "Thermal Model Development for LabPET II Scanner Adapter Board Detector Module", Proceedings of the COMSOL Conference, pp. 1-5, (Oct. 2015).
- [9] Sayde, M, Lakhssassi, A, Bougataya, M, Terkawi, O, & Blaquiere, Y, "SoC systems thermal monitoring using embedded sensor cells unit", In Circuits and Systems (NWSCAS), 55th IEEE International Midwest Symposium, pp. 1052-1055, (Aug. 2012).
- [10] Lakhssassi, A, Bougataya, M, Boustany, C, & Massicotte, D, "Thermal stress monitoring using gradient direction sensors", In Circuits and Systems (NEWCAS-TAISA), 6th IEEE International Northeast Workshop, pp. 177-180, (June. 2008).
- [11] Lakhssassi, A, M, Bougataya, "VLSI Thermal Analysis and Monitoring", In-Tech, Kirchengasse, A-1070 Vienna, Austria, pp. 441-456, (2009).
- [12] Lopez-Buedo, S, Garrido, J, & Boemo, E. I, "Dynamically inserting, operating, and eliminating thermal sensors of FPGA-based systems", IEEE Transactions on components and packaging technologies, pp. 561-566, (2002).
- [13] Bougataya, M, Lakhsasi, A, Savaria, Y & Massicotte, D, "Thermomechanical Stress Analysis of VLSI devices by partially coupled finite element methods", IEEE Proceedings; ISBN, pp. 509-513, (May. 2004).