An Automated Surveillance System based on Multi-Processor System-on-Chip and Hardware Accelerator

Mossaad Ben Ayed
College of Science and Humanities at AlGhat, Al Majmaah University, Kingdom of Saudi Arabia
Sfax University, Tunisia

SabeurElkosantini
College of Engineering, King Saud University
Kingdom of Saudi Arabia

Mohamed Abid
National School of Engineers of Sfax
University of Sfax,
Tunisia

***Abstract*—The video surveillance, such as an example of security system presents one of the powerful techniques used in advanced systems. Manual vision which is used to analyze video in the traditional approach should be avoided. An automated surveillance system based on suspicious behavior presents a great challenge to developers. The detection is encountered by complexity and time-consuming process. An abnormal behavior could be identified by different ways: actions, face, trajectory, etc. The characteristics of an abnormal behavior still presents a great problem. This paper proposes a specific System On Chip architecture for surveillance system based on Multi-Processor (MPSOC) and hardware accelerator. The aim is to accelerate the processing and obtain a reliable and accelerated suspicious behavior recognition. Finally, the experiment section proves the opportunity of the proposed system in terms of performance and cost.**

***Keywords*—Surveillance system; suspicious behaviors; multi-processor; accelerator; architecture**

I. INTRODUCTION

Nowadays, our lifetime is widely conditioned by different surveillance systems. All of them are increasingly monitored by computers. The main goal of surveillance system is identifying suspicious or undesirable behaviors such as thefts and looting with intent [1]. By definition, an abnormal action or behavior represents a suspicious behavior which could menace human life by different way as freedom, privacy, health, and properties [2]. Developers propose three essential steps (see Fig. 1) to recognize the suspicious behavior: object detection, tracking, and behavior exploration.

The first challenge was to define models to recognize a suspicious behavior. An anomalous behavior did not represent a simple action or behavior, but it is defined by some simple actions which present a complex behavior. Therefore, a suspicious behavior did not have a standard pattern and the recognition phase is challenged by the accuracy of the abnormal detection. Different related works are presented in the next section. They aimed to find an automated method to analyze suspicious behavior and to replace traditional monitors.

The detection of an object presents the first step in suspicious behavior recognition system which the whole system depends on it to ameliorate the recognition rate. A comparison among the main background subtraction methods is used to detect objects.

Then the tracking step is essential to define trajectory or behavior kind/type. Several algorithms are used in literature but the results are not always satisfactory [3].

This paper focuses on a specific case: detect the attempt of theft or scam in the case of Automated Teller Machine (ATM) security surveillance. This detection is performed by the exploration of a tracking and squatting action.

The second challenge was the design of a real-time surveillance system. It is known that video/image processing requires a specific architecture to obtain real-time results. In this paper, we present different techniques used to accelerate speed execution and we propose an attempt based on Data-driven Error Correcting Output Coding (DECOC) classifier to ensure the real-time execution.

To sum up, existing surveillance systems suffer from several issues:

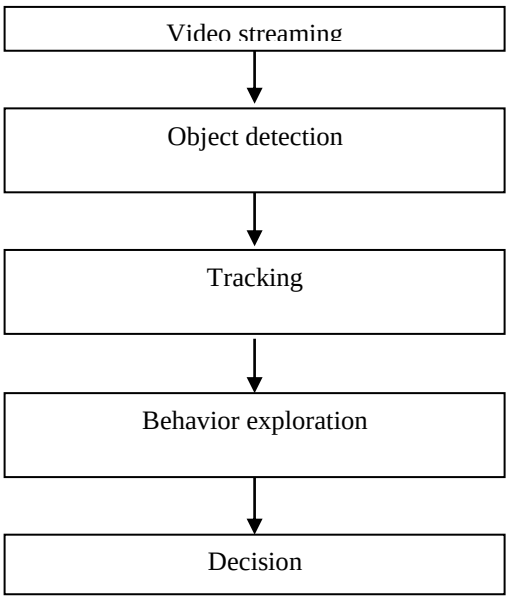


Fig. 1. Suspicious behavior's recognition steps.

1) The most traditional method of surveillance is based on manual/visual detection [4].

2) Most of today's surveillance is not used to prevent an incident but it is only used to identify what has already happened [5].

3) Most of surveillance systems suffer from no real-time detection of suspicious behavior. This problem is due to the complexity of algorithm [5].

4) Surveillance system violates the privacy of citizens. For example, in the USA, many groups such as NSA "National Security Agency", are against the use of surveillance system in public area [6].

In the light of this brief introduction on suspicious behavior based on surveillance system, this paper purports to contribute to the following tentative proposals:

1) Proposes an embedded intelligent camera for real-time execution. The intelligent camera ensures the privacy of citizens because all the treatments will be done in camera.

2) Applies the proposed design with respect to ATM system.

The present paper will be planned as follows:

The related work will be discussed in Section 2. Section 3 presents the basic concepts in terms of algorithm for surveillance system. Section 4 proposes a special design using MPSOC approach and hardware accelerator. The experimental results and accuracy analysis are exhibited in Section 5. Finally, Section 6 concludes the paper.

II. Related Work

The recognition of activities is targeted by multitude applications, especially suspicious behavior. Therefore, the presented field presents a point of interest for several researchers. In literature, conducting studies attempt to define the characteristics of an anomalous behavior and propose different techniques to analyze the detected behavior [2]. This section is divided into two parts: 1) literature review for the suspicious behavior recognition algorithm; 2) literature review for real-time architecture for surveillance system.

A. Suspicious Behavior Recognition Algorithms

Video surveillance systems get through especially three phases in literature. The first phase uses analog Closed-Circuit Television (CCTV) and the automation is little exploited (1960-1980). The second phase is based on computer vision using digital CCTVs (1980-2000). From 2000, the third phase is based on semi-automated video-surveillance systems [7]. As mentioned in the previous section, each suspicious behavior recognition is essentially composed of three steps: object detection, tracking, and behavior exploration.

1) There is a huge number related to objects detection, but algorithm still suffers from the complexity due to different specific situations. One of the most used methods for object detection is the subtraction of the background [8], [9]. Other works based on the last method are improved by formulated technique [10]. Multi-layer background subtraction which represents another method based on color and texture [11]. Second works are based on segmentation algorithms [12].

As a conclusion, we can say that the object detection is well done using subtraction method with the background [13].

2) Tracking methods are widely described in previous works. But these works still suffer from low accuracy because of the difficulty of generic algorithms. Tracking object system is used in many fields as: crowded environment [14], traffic situation [15] and maritime surveillance [16]. In the field of surveillance, the essential goal of the tracking object is to analyze or to extract the human behavior: trajectory, gesture, event [13], [17], [18].

3) Hierarchical methods and single layered methods are the two principle categories of the suspicious behavior recognition algorithms [2], [19]. The first is suitable for gesture recognition and the second is adopted for complex activities (Fig. 2).

4) Based on the model of the human activities, single layered methods are divided into: space time methods [2], [20]-[23] and sequential methods [2], [24]-[26].

In the space time method, the video is composed of a set of frames. Indeed, the local description based on trajectories extraction was used in recognizing behavior [2].

While in sequential method, the video is considered as a sequence of observation. Indeed, exemplar based methodologies is used for recognition [2].

Statistical methods [27], description-based methods [29], [30], and syntactic methods [28] present the constituent of hierarchical methods [2].

But all the previous works do not respect the real-time exigence due to the enormous amount of computation required [31].

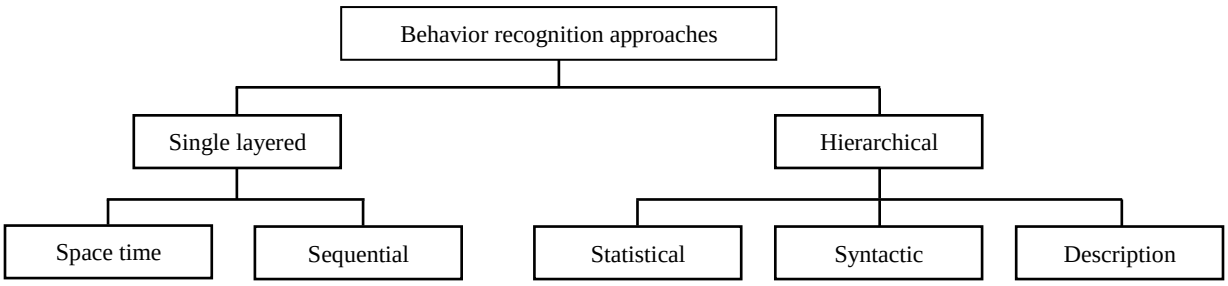


Fig. 2. Different behavior recognition approaches.

B. Real-time Detection based on Hardware Acceleration

The video processing is faced with not only the complexity of recognition algorithms but also the complexity of hardware architecture. Recognition algorithms request specific and advanced hardware components to avoid the loss of information and the non-real-time execution. [5].

There are various works of research that propose an advanced architecture in the field of video-surveillance. In [32] a co-design strategy is adopted with Field-Programmable Gate Array (FPGA) to ensure automated video surveillance in the case of the object detection.

Other works focus on embedded cameras for tracking systems [33], [34].

In [32], [35], [36], advanced designs are proposed to accelerate the detection of human motion.

This brief review attempted to show the principle challenges faced by surveillance systems especially the low accuracy of tracking and the non-real-time detection.

The present paper proposes an accelerated architecture for suspicious behavior.

III. Basic Concepts: Object Detection and Tracking

Object detection and tracking is the main purpose of any surveillance system. In this section, a brief survey about different used algorithms is presented. Its main goal is to make a comparison between methods and purposes. In literature, several algorithms of object detections and tracking was presented. In this section, some shortcomings and limitations were discussed.

Wang et al., [37] propose Incremental Multiple Principle Component Analysis (MPCA) algorithm for detection and tracking. Based on the time sequence, this method manages the variation of image's streams. To ensure online learning, a dynamic tensor defined by object's geometric presentation is used. It aims to find the relationship between image's matrices. Then Bays' interference framework is applied. Eigen tracking algorithm is modeled as a learning method. But this algorithm suffers from non-real-time execution [44].

Babenko et al. [38], propose a novel algorithm named Frag Track (FT). This algorithm tries to track an object from video advance. The object is represented by multiple fragments of an image. FT algorithm determines the histogram of an object in every position and each position is compared to histogram of the original object. The integral datagram structure is used by FT algorithm. It determines multiple regions based on the extraction result of the histogram. FT algorithm overcomes essentially three problems. First, it reduces the cost of computation. Second, FT uses pixel intensities based on spatial distribution. Third, FT occurs the partial occlusions [44].

Wang et al. [39], combine two algorithms to ensure object detection: Local Binary Pattern (LBP) and Histogram of Oriented Gradients (HOG). The proposed algorithm attempts to remove partial occlusions. This is ensured by using global and part detectors which scans the whole frames and the local regions. The mean shift technique is applied using maximum likelihood method to remove occlusions [43].

Co-Training Framework of Generative and Discriminative Trackers algorithm is proposed by Dinh et al. [40]. Authors propose the last algorithm to improve the detection of occlusion regions. A low dimension sub space is used by generative model to encode variation. And a Support Vector Machine (SVM) combined with HOG is used to provide discriminative model [44].

Grabner et al., [41] propose Semi Supervised Support Vector Machines (SSSVM) algorithm. This method tracks any object found in background and foreground in the frame. A semi supervised classifier used by the co-training framework, combines object's features to treat a new sample. This process provides an easy object detection and an easy separation with the background [44].

SVM is a complete computational procedure described in [42] and [43] with full details. It follows five process. In the first step, the SVM vectors with τ generation ensures training. Secondly, it looks for the input image. Thirdly, the SVM resize the image and apply normalization step. Fourthly, it starts classification. Finally, a filtration step is applied to decrease noise [45].

Equation (1) presents the model of the classification algorithm:

$$\sum_i \propto_i K(X_x, X_i) \geq \sum_i \propto_i K(X_s, X_i) = \tau \qquad (1)$$

Where the sphere radius is presented by τ. The supportive vectors derived in a training step are X_s and $\propto_i$. X_x is an input pixel.

The classifier compares the input pixel with all the support vectors. Then it determines if the input pixel belong to the inside of the sphere. A Gaussian kernel was used for implementation [45].

$$K = e^{-\gamma \left\| X_i - X_j \right\|^2} \qquad (2)$$

Where γ is a propagate of the kernel.

SSSVM algorithm solves all drawbacks occurred from the previous algorithms. It provides mainly a robust tracking. Furthermore, it combines between generative and discriminative model to track the object. Moreover, SSSVM mange easily the object types [43].

In the light of this brief review, algorithms based on SVM provide more accuracy than other detections and tracking algorithms. In the next section, a complete HW description will be described with sufficient details.

IV. Proposed Surveillance System: Modeling and Simulation

Embedded system is used in different fields as industries, surveillance, smart cities, intelligent systems, etc. There are several environments for modeling and simulation depending on level description and field system.

Architecture based on FPGAs boards presents an attractive platform for surveillance system not only to ensure real-time exigence but also to support the complexity of used algorithms.

The proposed architecture is based on multi-processor approach. FPGA offers flexibility to implement a specific architecture based on MPSOC in a single chip.

Fig. 3 shows the block diagram of the proposed hardware architecture. A pipelined multi-processor is used to speed up execution and to improve the precision computation. The proposed architecture is composed of three main functional blocks: Object detection Unit, Tracking Unit and Behavior exploration application. The first and the second are hardware components and they will be supported by a special purpose architecture described in Fig. 5. The third is a software application written in C language and executed by the principal processor of the controller unit.

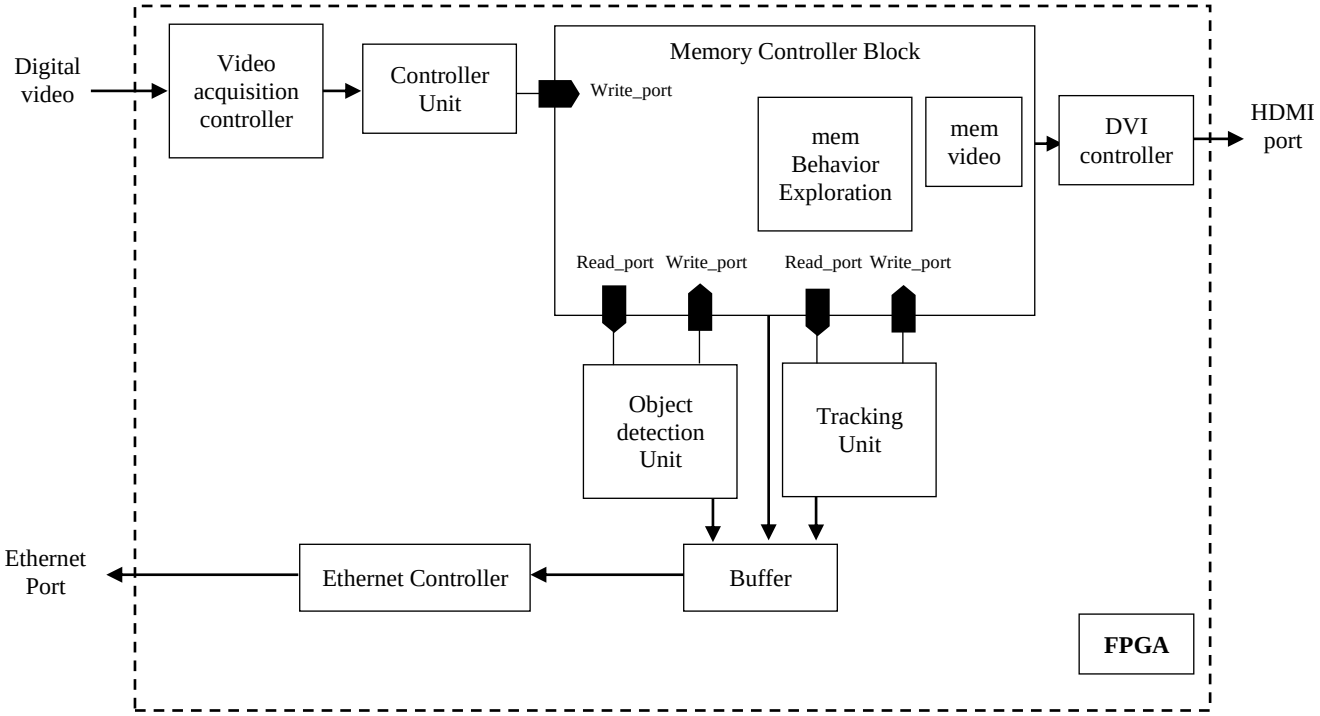


Fig. 3. Block diagram of the architecture.

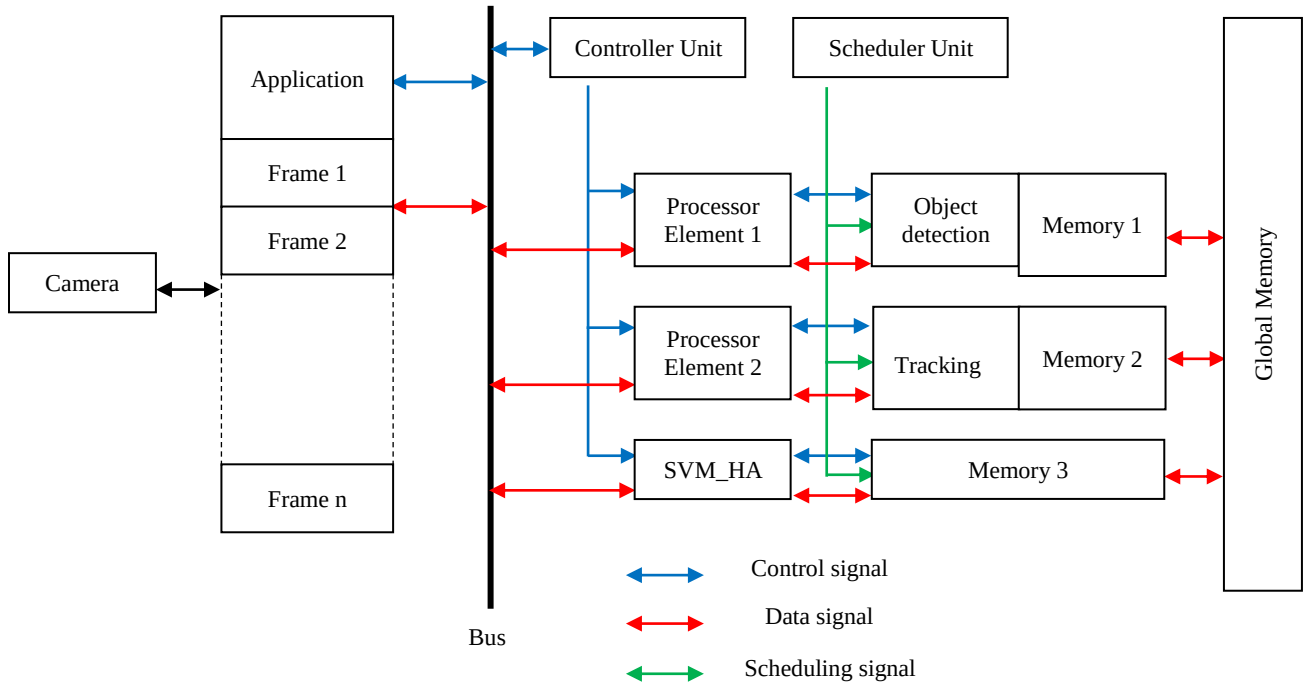


Fig. 4. Multi-processor based SVM Hardware Accelerator architecture for surveillance system.

The memory controller block is supported by an external DDR2 memory interface. It contains five ports three of which are used for writing and the rest is used for reading. Buffers are used to avoid frame artifacts.

The Controller unit represents the main component in the proposed design. It ensures different services:

- Divides frame into three slices.
- Arbitrates the access processors elements to/from memory.
- Manages processor elements status: idle, stopped, started, and running.
- Executes the application code of the behavior exploration.

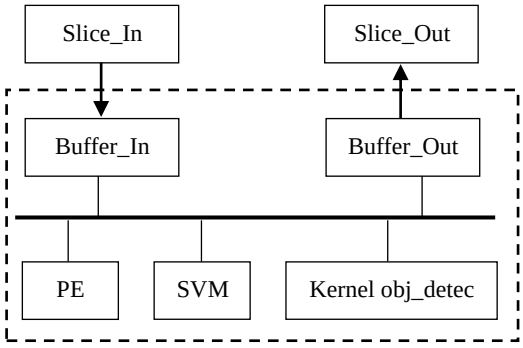
The internet interface is tied to the computer. This interface is added to visualize operations saved in the buffer.

The High-Definition Multimedia Interface (HDMI) is added to display output and verify the accuracy of the proposed architecture. Fig. 4 shows the kernel architecture.

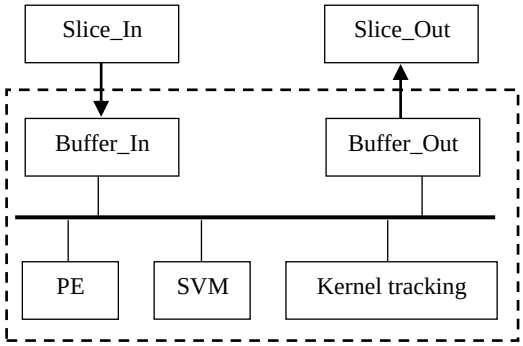
The proposed MPSOC architecture belongs to Single Instruction Multiple Data (SIMD) field [42]. The communication between different components is ensured by bus based on three signals: control signal, data signal, and scheduling signal. The scheduling unit manages slices in relation to kernels. The SVM_HA is a hardware accelerator described in Fig. 6.

Fig. 5 shows the architecture of object detection (a) and tracking (b). The proposed is a MPSOC approach based on Processor Element (PE) coupled with a SVM hardware accelerator. It aims to speed-up the classification step and respects real-time constraints. The kernel performs the main function and collaborates with SVM hardware accelerator.

Fig. 6 shows the block diagram of SVM Hardware accelerator composed by classification part with collaboration of an internal memory. Supportive Vectors are fetched from an external memory.



(a) Block diagram of object detection unit.



(b) Block diagram of tracking unit.

Fig. 5. Block diagram of processing unit.

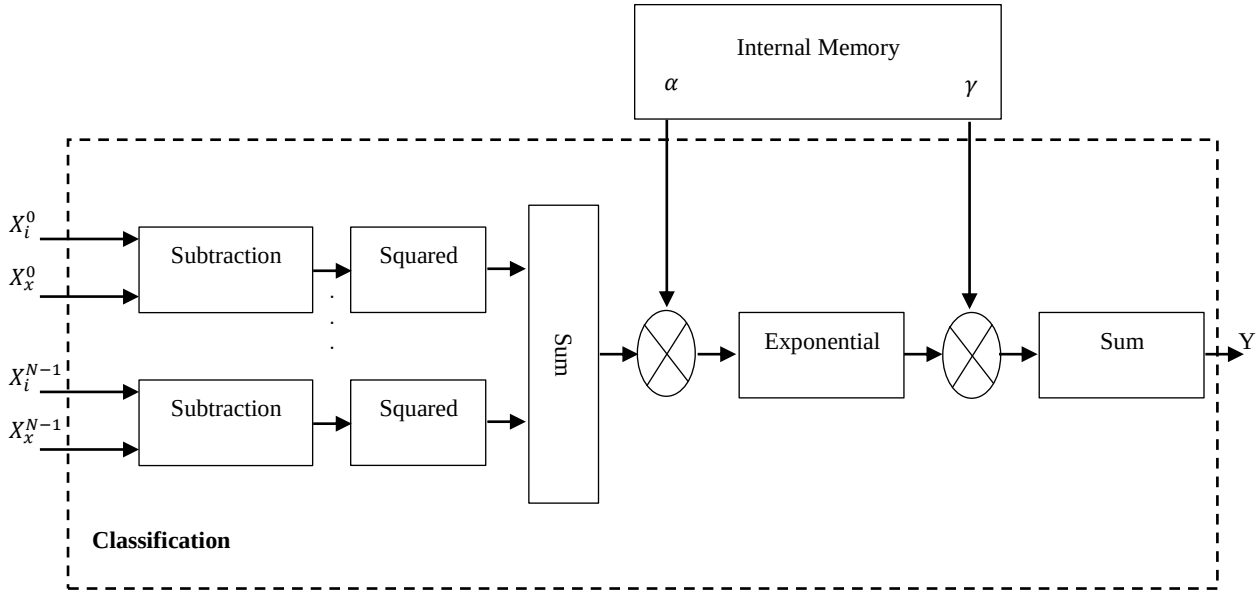


Fig. 6. Block diagram of SVM hardware accelerator.

V. Experiment Results

The implementation of the surveillance system using a hybrid architecture based on multi-processor and SVM based on a hardware accelerator is discussed in this section.

The proposed architecture in the previous section is implemented on an Altera DE2-115 board shown in Fig. 7 [42]. The FPGA reads the video stream from the USB camera Microsoft LifeCam Studio Q2F-00016 (see Fig. 8) with a resolution of 640 x 480 pixels. The purpose of this work is to obtain a real-time execution of the surveillance system using two NIOS II processors, hardware accelerator, and distributed memory.

In this work, detection object design and tracking design were written in VHSIC Hardware Description Language (VHDL) and were synthesized from a Register Transfer Level (RTL) model. Behavior exploration algorithm has written in C language. Then algorithm's optimization is applied to support the embedded MPSOC model.

The FPGA platform involves 32 bits NIOS II processor, 64 KB of on-chip Random Access Memory (RAM) for buffers, and 32 KB of on-chip RAM for behavior exploration as a software application.

To summarize, our design involves two NIOS II soft-core processors, a hardware accelerator, and a shared memory which present the design kernel. Control, data, and scheduling signals are ensured by the AVALON bus[1]. The design kernel's clock is running at 100 MHz. The AVALON bus is clocked at 50 MHz. The video acquisition controller is clocked at 73.6 MHz, the HDMI controller at 25 MHz, and the Ethernet controller at 125 MHz.

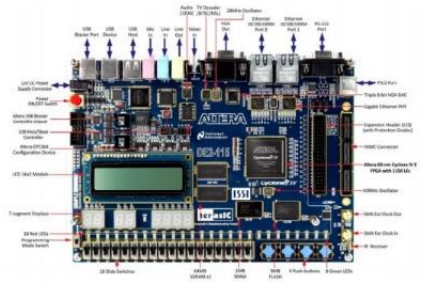


Fig. 7. DE2-115 Board.

Fig. 8. Microsoft LifeCam Studio camera.

[1] http://www.ee.ryerson.ca/~courses/coe608/labs/DE2_115_User_Manual.pdf.

TABLE I. FPGA Occupation

Resource Type	Logic elements	Total memory bits	DSP elements
Object detection unit	4752/39600 (12%)	499323/1161216 (43%)	0/252 (0%)
Tracking Unit	1188/39600 (3%)	220631/1161216 (19%)	0/252 (0%)
Behavior Exploration module	0/39600 (0%)	232651/1161216 (20%)	58/252 (23%)

TABLE II. Resources and Space Report

Resource type	Occupation	Rate
Combinational ALUT	101990/424960	24%
Memory ALUT	63/212480	0.29%
Logic Registers	89241/424960	21%
Total Pins	302/888	34%
Total block memory bits	17411604/21233664	82%
DSP block	133/1024	13%
PLL	2/8	25%

The resource requirements for each VHDL entity are indicated in Table 1. A Digital Signal Processor (DSP) element is the main processor type of the controller unit.

The FPGA occupation report proves that the configuration choices are selected to suport the specific requirements of the proposed application. The application uses 5940 logic elements inside the FPGA. The total blocks memory bits provided by the board is equal to 21233664. Based on results shown in Table 2, 24% of logic elements on FPGA is used by the design and 82% of memory is occupied.

Timing Analyzer tool evaluates the real-time performance of the system based on results of each processing step. The processing time is computed in microseconds. Table 3 indicates the time delay between two consecutive frames.

The results prove that the total processing time is about 81.140 ms. Therefore, the proposed system could run at 120 frames per second. This time delay presents much opportunity to speed-up execution time and ensures real-time processing.

TABLE III. The Average Computation Time by Frame Processing.

Processing step	Number of the points	Execution time (µs)
Object detection	841	584.346
Tracking	307	203.817
Behavior exploration	4093	80351.849

TABLE IV. The Dissipation Power of the FPGA Resource

Resources	Power (mW)
Memory controller	342
PLL	156
Detection object unit	143
Tracking unit	98
Ethernet controller	14
Video acquisition	6
Video display	9
Input/output blocks	406
Clock network	189
Leakage	85
Total	1448

Based on results of the power analysis and optimization tool, the entire system spends 1.448 W of power, where 768 mW are dissipated by our design, as mentioned in line one of the Table 4. This power dissipation is overpowered by the memory controller (342 mW). 426 mW presents the used power by all the processing modules. The total power dissipation (680 mW) indicated in line two in Table 4 presents the complete setup power. It is composed by the FPGA, Ethernet physical I/O chip and DDR2 external memory.

VI. Conclusion

This paper sums up the different automated surveillance system in the literature. The goal is to obtain a reliable detection of suspicious behavior with respect to the real-time constraint for ATM system. This successful attempt proposes a hybrid architecture based on multi-processor and hardware accelerator to speed-up the processing time.

The presented special-purpose hardware architecture for surveillance system was performed. The implanted prototype achieves low-cost in terms of FPGA scales. The accuracy has a double precision in comparison with software implementation. The frame rate of the prototype is 120fps, and the overpowered is 768mW.

The discussed results of the previous section prove the special architecture based not only on MPSOC approach but also on SVM-based Hardware Accelerator. The different performance features ensure accuracy with a real-time exigency.

In future work, the system will be extended to implement multi-camera in the context of Internet of Things (IOT) application.

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